

## **PART II**

### **A/D AND D/A CONVERTERS**



# Chapter Seven

## Understanding Converters

A/D converters translate from analog measurements, which are characteristic of most phenomena in the “real world,” to digital language, used in information processing, computing, data transmission, and control systems. D/A converters are used in transforming transmitted or stored data, or the results of digital processing, back to “real-world” variables for control, information display, or further analog processing.

### 7.1 BINARY CODES AND CONVERSION RELATIONSHIPS

#### 7.1.1 ANALOG QUANTITIES

Analog input variables, whatever their origin, are most frequently converted by transducers into voltages or currents. These electrical quantities may appear as fast or slow “dc” continuous direct measurements of a phenomenon in the time domain, as modulated ac waveforms (using a wide variety of modulation techniques), or in some combination, with a spatial configuration of related variables to represent shaft angles. Examples of the first are outputs of thermocouples, potentiometers on dc references, and analog computing circuitry; of the second, “chopped” optical measurements, ac strain gage or bridge outputs, and digital signals buried in noise; and of the third, synchros and resolvers.

The analog variables to be dealt with in this chapter are those involving “dc” voltages or currents representing the actual analog phenomena. They may be either wideband or narrow-band. They may be either scaled from the direct measurement, or subjected to some form of analog pre-processing, such as linearization, combination, demodulation, filtering, sample-hold, etc. As

part of the process, the voltages and currents are “normalized” to ranges compatible with assigned converter input ranges. Ways and means of accomplishing appropriate pre-processing, including floating-point scaling, are discussed in the chapters on applications and system accessories. Analog output voltages or currents from D/A converters are direct and in normalized form, but they may be subsequently post-processed (e.g., scaled, filtered, boosted, etc.).

This chapter does not include the conversion of signals from resolvers and synchros—widely used in some control applications. Relevant material on this topic will be found in Chapter 14.

### 7.1.2 DIGITAL QUANTITIES

Information in digital form is represented by arbitrarily fixed voltage levels referred to “ground,” either occurring at the outputs of logic gates, or applied to their inputs. The digital numbers used are all basically binary (in the sense of either-or); that is, each “bit,” or unit of information has one of two possible states. These states are “off,” “false,” or “0,” and “on,” “true,” or “1.”

*Words* are groups of levels representing digital numbers; the levels may appear simultaneously in *parallel*, on a bus or groups of gate inputs or outputs, *serially* (or in a time sequence) on a single line,\* or as a sequence of parallel bytes (i.e., “byte-serial”) or nybbles (small bytes). For example, a 16-bit word may occupy the 16 bits of a 16-bit bus, or it may be divided into two sequential bytes for an 8-bit bus, or four 4-bit nybbles for a 4-bit bus.

Although there are several systems of logic, the most widely used choice of levels are those used in TTL (transistor-transistor logic), in which positive *true*, or 1, corresponds to a minimum output level of +2.4V (inputs respond unequivocally to “1” for levels greater than 2.0V); and *false*, or 0, corresponds to a maximum output level of +0.4V (inputs respond unequivocally to “0” for anything less than +0.8V). A unique parallel or serial grouping of digital levels, or a *number*, or *code*, is assigned to each analog level which is quantized (i.e., represents a unique portion of the analog range). A typical digital code would be this array:

1 0 1 1 1 0 0 1

It is composed of eight bits. The “1” at the extreme left is called the “most significant bit” (MSB, or Bit 1), and the one at the right is called the “least significant bit” (LSB, or bit *n*: 8 in this case). The meaning of the code, as either a number, a character, or a representation of an analog variable, is unknown until the *code* and the *conversion relationship* have been defined.

\*In serial data transmission, if the levels return to ground between successive bits, they are denoted RZ (return-to-zero); if they change only when the leading or trailing edge of a clock pulse is present, and remain until the next such edge, they are denoted NRZ (non-return-to-zero).



### 7.1.3 BINARY CODE—INTEGERS AND FRACTIONS

The best-known code is *natural binary* (base 2). Binary codes are most familiar in representing integers; i.e., in a natural binary integer code having  $n$  bits, the LSB has a weight of  $2^0$  (i.e., 1), the next bit has a weight of  $2^1$  (i.e., 2), and so on up to the MSB, which has a weight of  $2^{n-1}$  (i.e.,  $2^n/2$ ). The value of a binary number is obtained by adding up the weights of all non-zero bits. When the weighted bits are added up, they form a unique number having any value from 0 to  $2^n - 1$ . Each additional trailing zero bit, if present, essentially doubles the size of the number.

In converter technology, because full scale (i.e., the converter's reference) is independent of the number of bits of resolution, a more useful coding is *fractional binary*, which is always normalized to full scale. Integer binary can be interpreted as fractional binary if all integer values are divided by  $2^n$ . For example, the MSB has a weight of  $1/2$  (i.e.,  $2^{(n-1)}/2^n = 2^{-1}$ ), the next bit has a weight of  $1/4$  (i.e.,  $2^{-2}$ ), and so forth down to the LSB, which has a weight of  $1/2^n$  (i.e.,  $2^{-n}$ ). When the weighted bits are added up, they form a number with any of  $2^n$  values, from 0 to  $(1 - 2^{-n})$  of full-scale. Additional bits simply provide more fine structure without affecting full-scale range. To illustrate these relationships, Table 7.1 lists the 16 permutations of 4-bits' worth of 1's and 0's, with their binary weights, and the equivalent numbers expressed as both decimal and binary integers and fractions.

When all bits are "1" in natural binary, the fractional number value is  $1 - 2^{-n}$ , or normalized full-scale less 1 LSB ( $1 - 1/16 = 15/16$  in the example). Strictly

Decimal Fraction	Code						Decimal Integer
	Binary Fraction	MSB ( $\times 1/2$ )	Bit 2 ( $\times 1/4$ )	Bit 3 ( $\times 1/8$ )	Bit 4 ( $\times 1/16$ )	Binary Integer	
0	0.0000	0	0	0	0	0 0 0 0	0
$1/16 = 2^{-4}$ (LSB)	0.0001	0	0	0	1	0 0 0 1	1
$2/16 = 1/8$	0.0010	0	0	1	0	0 0 1 0	2
$3/16 = 1/8 + 1/16$	0.0011	0	0	1	1	0 0 1 1	3
$4/16 = 1/4$	0.0100	0	1	0	0	0 1 0 0	4
$5/16 = 1/4 + 1/16$	0.0101	0	1	0	1	0 1 0 1	5
$6/16 = 1/4 + 1/8$	0.0110	0	1	1	0	0 1 1 0	6
$7/16 = 1/4 + 1/8 + 1/16$	0.0111	0	1	1	1	0 1 1 1	7
$8/16 = 1/2$ (MSB)	0.1000	1	0	0	0	1 0 0 0	8
$9/16 = 1/2 + 1/16$	0.1001	1	0	0	1	1 0 0 1	9
$10/16 = 1/2 + 1/8$	0.1010	1	0	1	0	1 0 1 0	10
$11/16 = 1/2 + 1/8 + 1/16$	0.1011	1	0	1	1	1 0 1 1	11
$12/16 = 1/2 + 1/4$	0.1100	1	1	0	0	1 1 0 0	12
$13/16 = 1/2 + 1/4 + 1/16$	0.1101	1	1	0	1	1 1 0 1	13
$14/16 = 1/2 + 1/4 + 1/8$	0.1110	1	1	1	0	1 1 1 0	14
$15/16 = 1/2 + 1/4 + 1/8 + 1/16$	0.1111	1	1	1	1	1 1 1 1	15

Table 7.1 Integer and fractional binary codes.

speaking, the number that is represented, written with an “integer point,” is 0.1111 ( $= 1 - 0.0001$ ). However, it is almost universal practice to write the code simply as the integer 1111 (i.e., “15”) with the fractional nature of the corresponding number understood: “1111”  $\rightarrow$   $1111/(1111 + 1)$ , or  $15/16$ .

For convenience, Table 2 lists bit weights in binary for numbers having up to 20 bits. The practical range for the vast majority of applications is about 16 bits; for numbers of bits than greater 20, continue to divide by 2.

BIT	$2^{-n}$	$1/2^n$ (Fraction)	“dB”	$1/2^n$ (Decimal)	%	ppm
FS	$2^0$	1	0	1.0	100	1,000,000
MSB	$2^{-1}$	1/2	-6	0.5	50.	500,000
2	$2^{-2}$	1/4	-12	0.25	25	250,000
3	$2^{-3}$	1/8	-18.1	0.125	12.5	125,000
4	$2^{-4}$	1/16	-24.1	0.0625	6.2	62,500
5	$2^{-5}$	1/32	-30.1	0.03125	3.1	31,250
6	$2^{-6}$	1/64	-36.1	0.015625	1.6	15,625
7	$2^{-7}$	1/128	-42.1	0.007812	0.8	7,812
8	$2^{-8}$	1/256	-48.2	0.003906	0.4	3,906
9	$2^{-9}$	1/512	-54.2	0.001953	0.2	1,953
10	$2^{-10}$	1/1,024	-60.2	0.0009766	0.1	977
11	$2^{-11}$	1/2,048	-66.2	0.00048828	0.05	488
12	$2^{-12}$	1/4,096	-72.2	0.00024414	0.024	244
13	$2^{-13}$	1/8,192	-78.3	0.00012207	0.012	122
14	$2^{-14}$	1/16,384	-84.3	0.000061035	0.006	61
15	$2^{-15}$	1/32,768	-90.3	0.0000305176	0.003	31
16	$2^{-16}$	1/65,536	-96.3	0.0000152588	0.0015	15
17	$2^{-17}$	1/131,072	-102.3	0.00000762939	0.0008	7.6
18	$2^{-18}$	1/262,144	-108.4	0.000003814697	0.0004	3.8
19	$2^{-19}$	1/524,288	-114.4	0.000001907349	0.0002	1.9
20	$2^{-20}$	1/1,048,576	-120.4	0.0000009536743	0.0001	0.95

Table 7.2 Binary bit weights or resolution.

The weight assigned to the LSB is the *resolution* inherent in numbers having  $n$  bits. The “dB” column represents the logarithm (base 10) of the ratio of the LSB value to unity (full scale), multiplied by 20, in the popular manner. Each successive power of 2 represents a change of 6.02dB [i.e.,  $20 \log_{10}(2)$ ] or “6dB/octave.”

In natural binary, the normalized numerical value of 1 0 1 1 0 0 1, an 8-bit code, would be

INTEGER:

$$\begin{array}{ccccccccccc}
 2^7 & + & 2^5 & + & 2^4 & + & 2^3 & + & 2^0 & & \\
 128 & + & 32 & + & 16 & + & 8 & + & 1 & = & 185
 \end{array} \quad (7.1)$$

FRACTION:

$$\begin{aligned}
& \frac{2^7}{2^8} + \frac{2^5}{2^8} + \frac{2^4}{2^8} + \frac{2^3}{2^8} + \frac{2^0}{2^8} \\
& \frac{128}{256} + \frac{32}{256} + \frac{16}{256} + \frac{8}{256} + \frac{1}{256} = \frac{185}{256} \\
& 2^{-1} + 2^{-3} + 2^{-4} + 2^{-5} + 2^{-8} \\
& \frac{1}{2} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{256} = \frac{185}{256} \\
& 0.5 + 0.125 + 0.0625 + 0.0313 + 0.0039 = 0.7227 \quad (7.2)
\end{aligned}$$

Bit numbering for microprocessor buses is based on whole numbers, not binary fractions. In such systems, the LSB is always Bit 0 (viz.,  $2^0$ ), the MSB is always Bit  $n-1$  (viz.,  $2^{n-1}$ ). Setting up a correspondence between the bit numbers used in words in the two systems,

Integral

Bit  $n-1$ : ( $2^{n-1}$ ), Bit  $n-2$ : ( $2^{n-2}$ ), . . . Bit  $n-n$  (i.e., 0): ( $2^0 = 1$ )

Fractional

Bit 1: ( $2^{-1}$ ), Bit 2: ( $2^{-2}$ ), . . . Bit  $n$ : ( $2^{-n}$ )

Thus, the bit number is equal to the logarithm of its weight, base 2, in integral binary, and to the negative of the logarithm of its weight in fractional binary.

Since the binary point is to the right of the LSB in integral binary, additional bits are always added to the left; integral binary numbers are said to be *right-justified*. On the other hand, in fractional binary, additional bits are always added to the right; fractional binary numbers are *left-justified*. This is of importance when a number is represented by two bytes, for example, when a 12-bit number must be placed on or retrieved from an 8-bit bus. If the binary number is left-justified, the more-significant byte has the first 8 bits, starting with the MSB, and the less-significant byte has the last 4 bits and 4 trailing zeros; for right-justified numbers, the more-significant byte has 4 leading zeros and the four more-significant bits, while the less-significant byte has the 8 less-significant bits.

#### 7.1.4 BASIC CONVERSION RELATIONSHIPS

Perhaps a graph is the most fruitful way of indicating in detail the relationship between analog and digital quantities in a conversion. Since there are two complementary conversion relationships to be discussed, two graphs must be plotted, one for A/D conversion, the other for D/A conversion.

Figure 7.1 shows the graph for an ideal 3-bit D/A converter. A 3-bit converter has 8 discrete coded levels, thus a total of 8 different inputs and 8 corresponding outputs, ranging from zero to  $\frac{7}{8}$  of "full scale." While full scale is not available digitally, it represents the reference quantity to which the analog

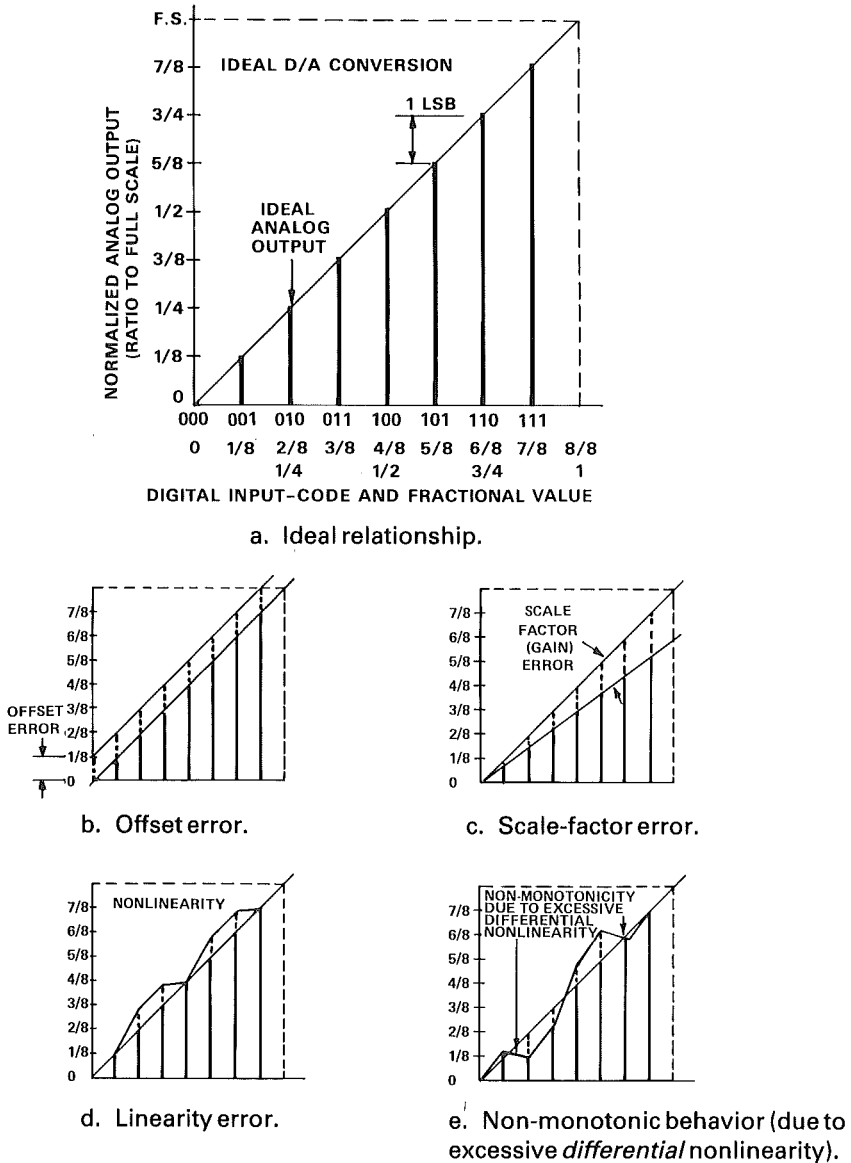


Figure 7.1. Conversion relationships in a 3-bit d/a converter, showing ideal relationship and typical sources of error.

variable is normalized (the *full-scale range* (or *span*) is 0 to 1, not 0 to  $7/8$ ). Since only the eight coded levels can exist, Figure 7.1 is plotted as a column graph.

Practical D/A converters have errors. For example, the zero column may not be exactly zero, giving rise to *offset error*. The extrapolated range from zero to F.S. may not be exactly as specified; this scale-factor error is often called *gain error*. The differences between the heights of adjacent bars may not be equal or changing uniformly (*nonlinearity*), and—in fact—if the *differential nonlinearity* (difference between adjacent heights and 1 LSB) is sufficiently

negative, the device may be *non-monotonic* (one or more values of analog output may actually be less than the values corresponding to codes having smaller weight). Even if differential linearity errors are within specification, there may be—for example—a gradually increasing nonlinearity error that becomes large between half scale and full scale; errors of this kind are called *integral nonlinearity* errors. The above errors (and others), the means of specifying and testing them, and some of the design techniques for keeping them small, are discussed in chapters 8, 9, 10, and 11.

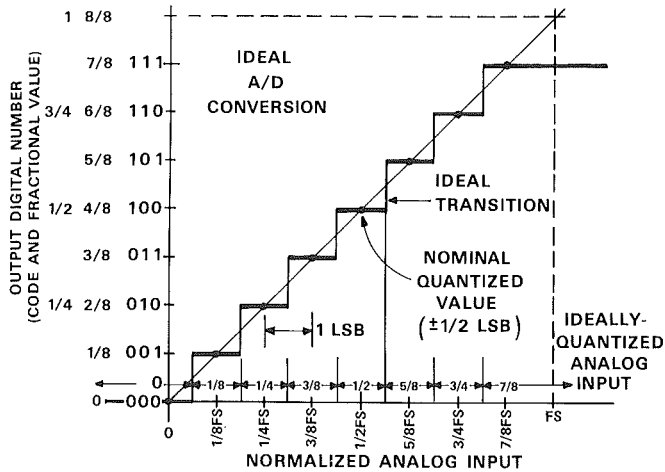
To visualize the ideal performance of converters having larger numbers of bits, one may intensify this pattern by interpolating additional columns between the columns of this graph. For example, a fourth bit would require 8 additional columns with heights halfway between the levels indicated. The value of the LSB would be F.S./16, and the maximum value would be  $\frac{7}{8} + \frac{1}{16} = \frac{15}{16}$  F.S. The next bit would interpolate 16 additional columns, the new LSB would be F.S./32, and the maximum value would be  $\frac{31}{32}$ , etc. The straight line connecting the tops of the columns is the locus of the *envelope* of the ideal conversion relationship.

Figure 7.2 shows the graph for an ideal 3-bit A/D converter. Since all values of the analog input are presumed to exist, they must be *quantized* by partitioning the continuum into 8 discrete ranges. All analog values within a given range are represented by the same digital code, which generally corresponds to the nominal mid-range value. These mid-range values correspond to the bar heights of the D/A converter.

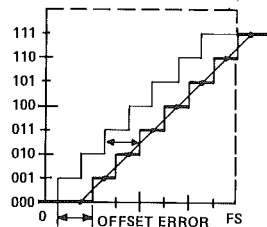
There is, therefore, in the A/D conversion process, an inherent *quantization uncertainty* of  $\pm \frac{1}{2}$  LSB, in addition to the conversion errors analogous to those existing for the D/A converter. The only sure way to reduce this quantization uncertainty—which is like a roundoff or truncation error—is to increase the number of bits of resolution. (There are, of course, statistical interpolation tricks that may be performed in the digital processing or in analog filtering following subsequent D/A conversion, which will fill in probable analog values for large, rapidly varying or repetitive signals, but they will do nothing to indicate the variations within a quantum for an apparently constant digital number.)

Since it is easier\* to determine the location of a *transition* than it is to determine a mid-range value, errors and settings of A/D converters are defined and measured in terms of the analog values at which transitions occur, in relation to the ideal transition values. Like D/A converters, A/D converters have offset error: the first transition may not occur at exactly  $+\frac{1}{2}$  LSB; scale-factor (or gain) error: the difference between the values at which the first transition and the last transition occur is not equal to (F.S.  $- 2$ LSB); and *linearity* error: the differences between transition values are not all equal or uniformly changing.

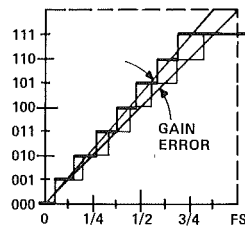
\*(using analog techniques)



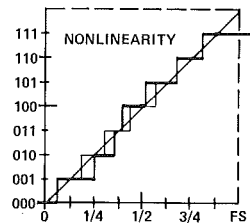
a. Ideal relationship.



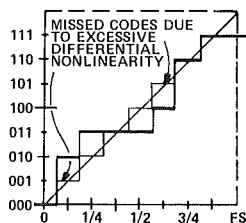
b. Offset error.



d. Linearity error.



c. Scale-factor error.



e. Missed codes.

Figure 7.2. Conversion relationships in a 3-bit a/d converter, showing ideal relationship and typical sources of error.

If the *differential linearity* error is large enough, it is possible for one or more codes to be missed (the counterpart of non-monotonic D/A conversion).

An important factor in the conversion relationship is the choice of “Full Scale,” the LSB magnitude, and the transition points. For a great many converters, full scale is in the vicinity of 10 volts: either exactly at 10V or at 10.24V. For 10V, the bit values are easily expressed as negative powers of 2, multiplied by 10; for 10.24V, the LSB can be expressed in “round” numbers, being a multiple or submultiple of 10mV.

Table 7.3 lists the LSB values, the “all 1’s” value (i.e., F.S. – 1 LSB), and the A/D converter transition values at  $\frac{1}{2}$  LSB (for zero adjustment) and all

No. of Bits <i>n</i>	10V Full Scale				10.24V Full Scale			
			A/D Transitions				A/D Transitions	
			To LSB (1/2LSB)	To All 1's (Volts)			To LSB (+ 1/2 LSB)	To All 1's (Volts)
1	5V	5.0	2.5V	2.5	5.12V	5.12	2.56V	2.56
2	2.5V	7.5	1.25V	6.25	2.56V	7.68	1.28V	6.40
3	1.25V	8.75	625mV	8.13	1.28V	8.96	640mV	8.32
4	625mV	9.38	312mV	9.07	640mV	9.60	320mV	9.28
5	312mV	9.69	156mV	9.53	320mV	9.92	160mV	9.76
6	156mV	9.84	78.1mV	9.76	160mV	10.08	80mV	10.00
7	78.1mV	9.92	39.1mV	9.88	80mV	10.16	40mV	10.12
8	39.1mV	9.961	19.5mV	9.941	40mV	10.20	20mV	10.18
9	19.5mV	9.980	9.77mV	9.970	20mV	10.220	10mV	10.21
10	9.77mV	9.990	4.88mV	9.985	10mV	10.230	5mV	10.225
11	4.88mV	9.9951	2.44mV	9.9927	5mV	10.235	2.5mV	10.232
12	2.44mV	9.9976	1.22mV	9.9964	2.5mV	10.2375	1.25mV	10.2362
13	1.22mV	9.9988	610μV	9.9982	1.25mV	10.2388	625μV	10.2382
14	610μV	9.9994	305μV	9.9991	625μV	10.2394	312μV	10.2391
15	305μV	9.99970	153μV	9.99955	312μV	10.23969	156μV	10.23953
16	153μV	9.99985	76μV	9.99977	156μV	10.23984	78.1μV	10.23976
17	76μV	9.99992	38μV	9.99988	78.1μV	10.23992	39.1μV	10.23988
18	38μV	9.999962	19μV	9.999943	39.1μV	10.239961	19.5μV	10.239941
19	19μV	9.999981	9.5μV	9.999971	19.5μV	10.239980	9.77μV	10.239970
20	9.5μV	9.999990	4.8μV	9.999985	9.77μV	10.239990	4.88μV	10.239985

Table 7.3 LSB and (FS – LSB) values for 10V and 10.24V conversion.

1’s (F.S. –  $1 \frac{1}{2}$  LSB, for scale factor adjustment) for resolutions to  $2^{-20}$ , for both 10V and 10.24V full scale. If full scale is 5V (also a popular value), simply divide the appropriate numbers by 2.

## 7.2 OTHER CODES

Although binary is the most commonly used code, there are a number of other popular codes used at system interfaces, depending on signal range and polarity, conversion technique, specially desired characteristics, and origin or destination of digital information.

### 7.2.1 BINARY-CODED DECIMAL (BCD)

This is a code in which each decimal digit is represented by a group of 4 binary-coded digits (or “quad”). In fractional BCD, the LSB of the most significant quad has a weight of 0.1, the LSB of the next has a weight of 0.01, the LSB of the next has a weight of 0.001, etc. Each quad has 10 permissible levels with weights 0 to 9. Group values in excess of 9 are not permitted. Table 7.4 gives examples of BCD coding for a variety of numbers between 0 and 0.99.

A/D converters with the BCD code are used primarily in digital voltmeters and panel meters, since each quad’s output may be decoded to drive a numeric display using the familiar decimal numbers. If the display is of a BCD digitally

Decimal Fraction	BCD Code	
	MSQ ( $\times 1/10$ )	2nd Quad ( $\times 1/100$ )
	$\times 8 \times 4 \times 2 \times 1$	$\times 8 \times 4 \times 2 \times 1$
0.00 = 0.00 + 0.00	0 0 0 0	0 0 0 0
0.01 = 0.00 + 0.01	0 0 0 0	0 0 0 1
0.02 = 0.00 + 0.02	0 0 0 0	0 0 1 0
0.03 = 0.00 + 0.03	0 0 0 0	0 0 1 1
0.04 = 0.00 + 0.04	0 0 0 0	0 1 0 0
0.05 = 0.00 + 0.05	0 0 0 0	0 1 0 1
0.06 = 0.00 + 0.06	0 0 0 0	0 1 1 0
0.07 = 0.00 + 0.07	0 0 0 0	0 1 1 1
0.08 = 0.00 + 0.08	0 0 0 0	1 0 0 0
0.09 = 0.00 + 0.09	0 0 0 0	1 0 0 1
0.10 = 0.10 + 0.00	0 0 0 1	0 0 0 0
0.11 = 0.10 + 0.01	0 0 0 1	0 0 0 1
:		
0.20 = 0.20 + 0.00	0 0 1 0	0 0 0 0
:		
0.30 = 0.30 + 0.00	0 0 1 1	0 0 0 0
:		
0.90 = 0.90 + 0.00	1 0 0 1	0 0 0 0
0.91 = 0.90 + 0.01	1 0 0 1	0 0 0 1
:		
0.98 = 0.90 + 0.08	1 0 0 1	1 0 0 0
0.99 = 0.90 + 0.09	1 0 0 1	1 0 0 1

Table 7.4 Examples of 2-digit BCD weighting.

transmitted or processed number, or if the input is via a thumbwheel switch, a D/A converter that responds to BCD may be used to furnish a base-10 analog output from its digital input.

BCD is somewhat wasteful of bits, in the sense that each BCD quad has  $10/16$  the resolution of a comparable natural binary quad. Table 7.5 shows the relative resolution capability.

Number of Bits	Least Significant Bit		Number of Binary Bits Needed For Same Resolution as BCD
	Binary	BCD	
4	0.062	0.1	4
8	0.0039	0.01	7
12	0.00024	0.001	10
16	0.000015	0.0001	14
20	0.000001	0.00001	17
24	0.0000002	0.000001	20

Table 7.5 Relative resolution of BCD and binary.

## OVERRANGING

Many BCD A/D converters have an additional bit with weight equal to full scale, in a position “more significant” than the MSB.

This additional bit provides a maximum of 100% “overrange” capability. Additional “super-significant” bits would provide binary 300% (2 bits) and 700% (3 bits) overrange capability (or extend the range to nearly 800% of the



BCD “full scale”). Depending on how it is presented, the overrange bit is used in digital voltmeters and panel meters either to provide additional resolution or to indicate that nominal full scale has been exceeded and that the visual reading may be erroneous.

Overrange bits need not be restricted to BCD. They are useful as “flags” in any conversion process for which an overrange input would given an ambiguous reading, or where an overrange input indicates anomalous analog system behavior. The overrange bit must of course be of suitable accuracy, since it is, in effect, the MSB.

### 7.2.2 GRAY CODE

In Gray codes, each bit represents a binary-weighted segment of the range, and each code corresponds to a unique location in the range; but the bit weights do not readily combine to form a binary magnitude. However, Gray codes are easily translatable into natural binary (Table 7.6):

Decimal Fraction	Gray Code				Binary Code			
0	<u>0</u>	0	0	0	0	0	0	0
1/16	<u>0</u>	0	0	<u>1</u>	0	0	0	1
2/16	0	0	<u>1</u>	<u>1</u>	0	0	1	0
3/16	0	0	<u>1</u>	<u>0</u>	0	0	1	1
4/16	0	<u>1</u>	1	<u>0</u>	0	1	0	0
5/16	0	<u>1</u>	1	<u>1</u>	0	1	0	1
6/16	0	1	<u>0</u>	<u>1</u>	0	1	1	0
7/16	0	1	<u>0</u>	<u>0</u>	0	1	1	1
8/16	<u>1</u>	1	0	<u>0</u>	1	0	0	0
9/16	<u>1</u>	1	0	<u>1</u>	1	0	0	1
10/16	1	1	<u>1</u>	<u>1</u>	1	0	1	0
11/16	1	1	<u>1</u>	<u>0</u>	1	0	1	1
12/16	1	<u>0</u>	1	<u>0</u>	1	1	0	0
13/16	1	<u>0</u>	1	<u>1</u>	1	1	0	1
14/16	1	0	<u>0</u>	<u>1</u>	1	1	1	0
15/16	1	0	<u>0</u>	<u>0</u>	1	1	1	1

Table 7.6 Comparison of 4-Bit binary and Gray codes. Underlined bits indicate changes as number increases.

In Gray code, as the number value changes, the transitions from one code to the next involve only one bit at a time. The bits that change as the numbers increase are underlined in the table.

The conversion from binary to Gray code occurs as follows: If the binary MSB is zero, the Gray code MSB will be zero. Then, continuing to read from MSB to LSB, each change produces a “1,” each non-change produces a “0.” For example, binary 1011 becomes 1110 in Gray code (1 → 1, 1-to-0 → 1, 0-to-1 → 1, 1-to-1 → 0). Another example: the 12-bit binary number

101111000101 becomes 111000100111. Figure 7.3 shows one way in which binary to Gray code conversion may be mechanized.

The conversion from Gray code to binary is just the reverse of the conversion from binary to Gray code: the binary MSB will be the same as the Gray code

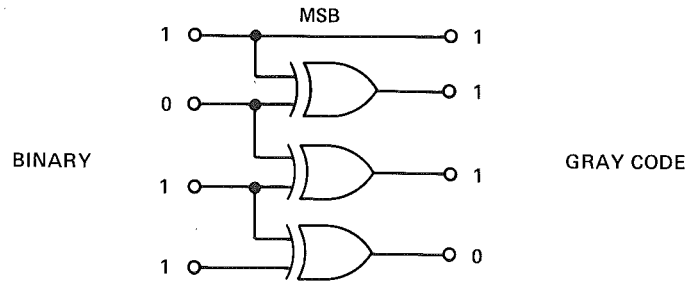


Figure 7.3. Binary-to-Gray code conversion using exclusive-or gates.

MSB. Then, continuing to read from MSB to LSB, if the next bit is 1, the next binary bit is the complement of the previous binary bit. For example, if the Gray code is 1110, the corresponding binary is 1011 (1  $\rightarrow$  1, 1  $\rightarrow$  1-to-0, 1  $\rightarrow$  0-to-1, 0  $\rightarrow$  1-to-1). Another example, the 8-bit Gray code 01110000 is 01011111 in binary. A mechanization of Gray code-to-binary conversion appears in Figure 7.4.

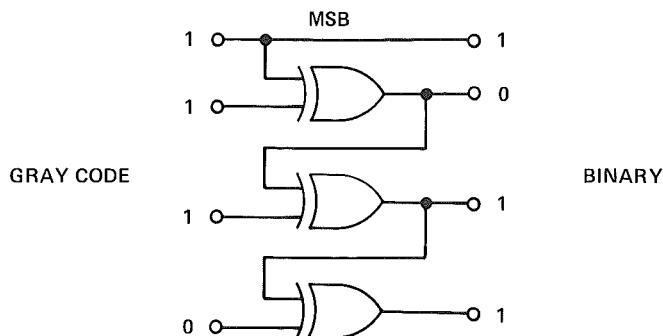


Figure 7.4. Gray Code-to-binary conversion.

Gray code is useful for shaft encoders (angle-to-digital converters) because the change of only 1 bit for each increment eliminates false intermediate codes that could occur in natural binary conversion. Here, for comparison, are Gray code and binary developed optical shaft encoders for 4-bit resolution.

Note that, with the Gray code converter, there is only one bit-change at each transition. If the edge of a shaded area is slightly out of line, the coding will be in error by a small fraction of an LSB. In the binary converter, *all four bits*

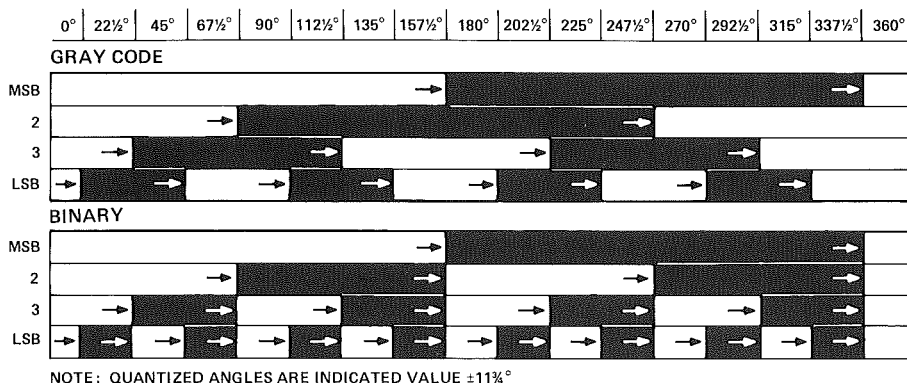


Figure 7.5. Gray vs. binary encoding.

*change at once* at the 180° and 360° transitions. If bit 2's shaded area were to end a little to the left of the 180° transition, the code, in a small region, would be 0011, indicating the 67½° range, or a fictitious progression from 157½° to 67½° to 180°. We leave the catastrophic implications of this to the reader.

The shaft encoder is a *simultaneous* converter: all bits appear at once and can be read in parallel at any time. An electrically equivalent form of simultaneous A/D converter, sometimes having a Gray code output, is the *flash* converter (see also Chapter 13). It employs a chain of biased comparators, the outputs of which provide a quantized indication of the analog input level: all comparators above it are 0, all comparators below it are 1. Multi-input gates then make the decisions necessary to obtain a parallel Gray code output. Such converters are quite fast, some being capable of producing 100 million or more meaningful conversions per second, but they require a number of comparisons that is a geometric function of the required resolution, (i.e.,  $2^n - 1$ ), as well as logic gates having large numbers of inputs.

A variation of this scheme, the cyclical converter, which also has Gray code output, uses fewer comparators, with more-accurate output states, but it requires more time to perform the conversion. It continuously tracks the analog input.

The use of Gray code in fast converters that provide continuous conversions has the same rationale as in the case of the shaft encoder. Any Gray code output value (for a 1-bit-accurate converter) that is latched into a register will always be within  $\pm 1$  LSB of the correct value, even if the latching occurs just as a bit is switching. With binary, however, where many bits can switch at a single transition, it is possible to latch in mid-flight, and, because of the "skew" between turn-on and turn-off speeds, lock in a false code. Sample-hold ahead of the conversion helps alleviate the situation in straight binary coding.

### 7.2.3 COMPLEMENTARY CODES

The actual mechanization of some forms of converters, (for example, early D/A converters using monolithic NPN quad current switches) required codes such as natural binary or BCD, but with all bits are represented by their complements. Such codes are called complementary codes.

In a 4-bit complementary-binary converter, 0 is represented by 1111, half-scale (MSB) by 0111, and full scale, less 1 LSB, by 0000. It can be easily obtained from the ["Q"] outputs of a register, of which "Q" is the normal output sense.

Similarly, for each quad of a BCD-coded converter, *complementary* BCD is the code obtained by representing all bits by their complements. In complementary BCD, 0 is represented by 1111, and 9 is represented by 0110. As an example, Table 7.7 lists the equivalents for 1 through 11 in complementary binary and complementary BCD (with overrange bit).

INT	Decimal Number		Natural Binary	Complementary Binary	BCD	Complementary BCD
	Fract. BIN	Fract. BCD				
0	0	0	0 0 0 0	1 1 1 1	0 0 0 0 0	1 1 1 1 1
1	1/16	1/10	0 0 0 1	1 1 1 0	0 0 0 0 1	1 1 1 1 0
2	2/16	2/10	0 0 1 0	1 1 0 1	0 0 0 1 0	1 1 1 0 1
3	3/16	3/10	0 0 1 1	1 1 0 0	0 0 0 1 1	1 1 1 0 0
4	4/16	4/10	0 1 0 0	1 0 1 1	0 0 1 0 0	1 1 0 1 1
5	5/16	5/10	0 1 0 1	1 0 1 0	0 0 1 0 1	1 1 0 1 0
6	6/16	6/10	0 1 1 0	1 0 0 1	0 0 1 1 0	1 1 0 0 1
7	7/16	7/10	0 1 1 1	1 0 0 0	0 0 1 1 1	1 1 0 0 0
8	8/16	8/10	1 0 0 0	0 1 1 1	0 1 0 0 0	1 0 1 1 1
9	9/16	9/10	1 0 0 1	0 1 1 0	0 1 0 0 1	1 0 1 1 0
10	10/16	10/10	1 0 1 0	0 1 0 1	1 0 0 0 0	0 1 1 1 1
11	11/16	11/10	1 0 1 1	0 1 0 0	1 0 0 0 1	0 1 1 1 0

Table 7.7 Complementary codes.

If a natural binary input were applied to a D/A converter coded to respond to complementary binary, the output would be in reverse order, i.e., zero output for all 1's, and F.S. - 1 LSB for all 0's.

The complementary codes discussed above involve complementing *all bits*, for convenience in implementing the conversion relationship using certain kinds of switches (i.e., those that respond to complementary logic). We could just as well have left the logic unchanged but redefined it as "negative true." However, for consistency in elucidation, we define all logic in terms of "positive true" TTL (or CMOS), as explained at the beginning of the chapter. It is important to understand that, for purposes of this discussion, these complementary codes have nothing to do with representation of the *analog polarity* (a matter that will be discussed next).

### 7.3 ANALOG POLARITY AND SCALING

So far, the conversion relationships mentioned have been unipolar (or nonpolar): the codes represent numbers, which in turn represent the normalized *magnitudes* of analog variables,\* without regard to polarity. A unipolar A/D converter will respond to analog signals of only one polarity, and a unipolar D/A converter will produce analog signals of only one polarity.

For any application, a converter must be used whose reference and switches (and specifications) are compatible with the desired analog polarity. If, for reasons of economy or availability, a converter is available having a predetermined polarity different from that desired, the overall function's polarity may be modified by operating on the analog signal before A/D conversion—or after D/A conversion—to invert or double its polarity, and also to perform any necessary scale changes, if range must be adapted, too.

#### 7.3.1 BIPOLAR CODES

For conversion of bipolar analog signals into a digital code that retains sign information, an extra bit, or sequence of bits, is necessary to indicate polarity. This extra “most-significant bit” doubles the analog range and halves the peak-to-peak resolution. In some cases, the sign bit is provided by re-interpreting the existing MSB, in which event the analog *range* may still be doubled, but the *resolution* is twice as coarse. For example, if a 10-bit converter's resolution is 1/1,024, for the range 0-10V, we may use a bipolar code having 11 bits,

Number	Decimal Fraction		Sign + Magnitude	Twos Complement	Offset Binary	Ones Complement
	Positive Reference	Negative Reference				
+7	+7/8	-7/8	0 1 1 1	0 1 1 1	1 1 1 1	0 1 1 1
+6	+6/8	-6/8	0 1 1 0	0 1 1 0	1 1 1 0	0 1 1 0
+5	+5/8	-5/8	0 1 0 1	0 1 0 1	1 1 0 1	0 1 0 1
+4	+4/8	-4/8	0 1 0 0	0 1 0 0	1 1 0 0	0 1 0 0
+3	+3/8	-3/8	0 0 1 1	0 0 1 1	1 0 1 1	0 0 1 1
+2	+2/8	-2/8	0 0 1 0	0 0 1 0	1 0 1 0	0 0 1 0
+1	+1/8	-1/8	0 0 0 1	0 0 0 1	1 0 0 1	0 0 0 1
0	0+	0-	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
0	0-	0+	1 0 0 0	(0 0 0 0)	(1 0 0 0)	1 1 1 1
-1	-1/8	+1/8	1 0 0 1	1 1 1 1	0 1 1 1	1 1 1 0
-2	-2/8	+2/8	1 0 1 0	1 1 1 0	0 1 1 0	1 1 0 1
-3	-3/8	+3/8	1 0 1 1	1 1 0 1	0 1 0 1	1 1 0 0
-4	-4/8	+4/8	1 1 0 0	1 1 0 0	0 1 0 0	1 0 1 1
-5	-5/8	+5/8	1 1 0 1	1 0 1 1	0 0 1 1	1 0 1 0
-6	-6/8	+6/8	1 1 1 0	1 0 1 0	0 0 1 0	1 0 0 1
-7	-7/8	+7/8	1 1 1 1	1 0 0 1	0 0 0 1	1 0 0 0
-8	-8/8	+8/8		1 0 0 0	0 0 0 0	

Table 7.8 Commonly used bipolar codes.

\*A/D converter input or D/A converter output.

with peak-to-peak resolution of  $1/2,048$  and range of  $\pm 10\text{V}$ , or retain a code having 10 bits, but “stretch” the range to  $\pm 10\text{V}$ , in which case the peak-to-peak resolution remains  $1/1,024$ , which doubles the magnitude of the LSB.

The most-often-used binary codes in bipolar conversion are: twos complement, sign-magnitude (magnitude plus sign), offset binary, and ones complement. Table 7.8 shows each of these codes expressed for 4 bits (3 bits plus sign). Generally, if the bus that a converter is connected to is wider than a right-justified byte, the sign bit in twos complement is repeated as many times as required to fill the remaining spaces to the left (e.g., on an 8-bit bus,  $-3/8$  in twos complement should be processed as if it were 1111 1101).

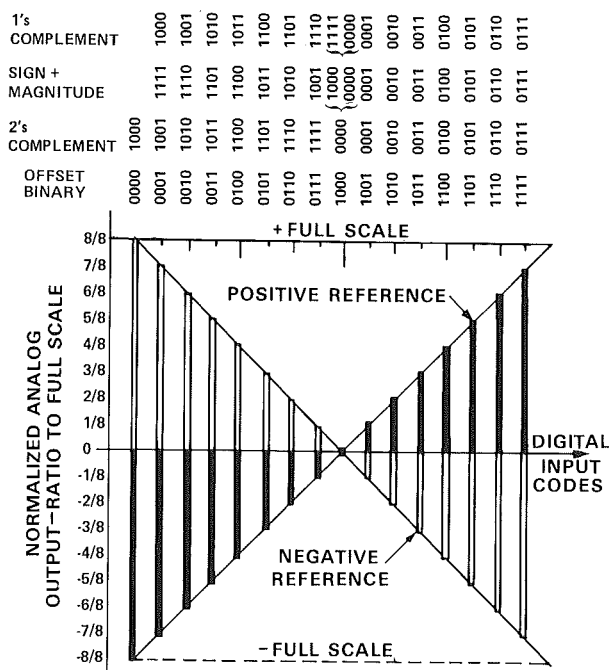


Figure 7.6. Ideal bipolar d/a conversion relationship for 4-bit (3-bit-plus-sign) offset-binary, twos-complement, sign-magnitude, and ones-complement codes.

Because the analog signal now has a choice of polarity, we must be careful about the relationship between the code and the polarity of the analog signal. “Positive reference” indicates that the analog signal\* increases positively as the digital number increases. “Negative reference,” on the other hand, indicates that the analog signal decreases towards negative full scale as the digital number increases. Conversion relationships for bipolar D/A and A/D converters are shown graphically in Figures 7.6 and 7.7.

\*Gray code is an exception. Since it is not quantitatively weighted, it can represent any arbitrary range of magnitudes of any polarity.

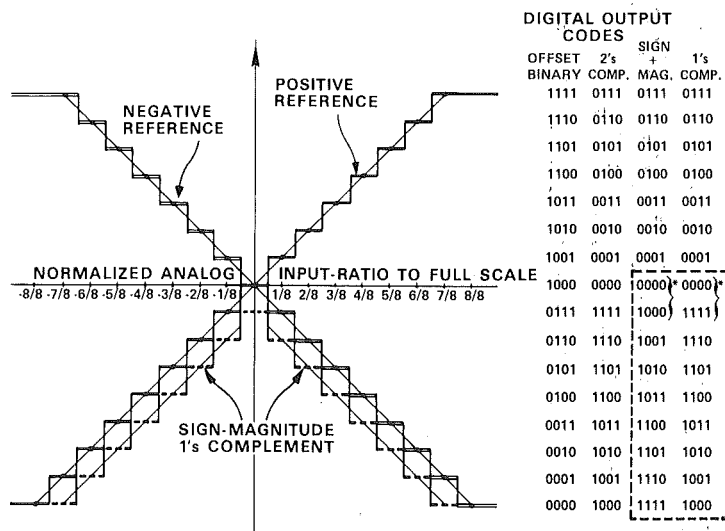


Figure 7.7. Ideal bipolar a/d conversion relationship for 4-bit (3-bit-plus-sign) offset-binary, two's-complement, sign-magnitude, and ones-complement codes.

*Sign-Magnitude* would appear to be the most straightforward way of expressing signed analog quantities digitally. Simply determine the code appropriate for the magnitude and add a polarity bit. It is used advantageously in D/A converters that operate in the vicinity of zero, where the application calls for smooth and linear transitions from small positive voltages to small negative voltages. As can be seen in the example in the table, it is the only binary code for which the three magnitude bits do not have a major transition (all 1's to all 0's, or equivalent) at zero. Sign-magnitude BCD is almost universally used for bipolar digital voltmeters (A/D converters).

It does have some shortcomings, though. In data-processing applications, the *other* codes are more-readily usable for computation with a minimum of translation. One of its problems is that it has two codes for zero. For this reason, sign-magnitude is harder to interface with digitally, because it requires processing by additional software and/or hardware.

*Offset binary* is the easiest code to embody with converter circuitry. An examination of the offset binary code for three bits plus sign will show that it is really a natural binary code for four bits, but the zero of the code is at negative full scale, the LSB is  $1/16$  of the bipolar range, and the MSB is turned on at analog zero. Therefore, to make an offset binary 3-bits-plus sign converter out of a 4-bit D/A converter having 0-to-10V full-scale range, we have only to double its scale factor (20V range), and offset its zero by one half of the full range ( $-10V$ ), an operation which is neither difficult nor expensive. Similarly, for an A/D converter, one would attenuate the input by one-half, and add a bias of one-half the full range.

\*When A/D converters with sign-magnitude or ones complement coding are required, the ambiguous zero must be handled appropriately.

Besides its ease of implementation, offset binary is compatible with computer inputs and outputs; it is easily changed to the more-computationally useful twos complement (just complement the MSB and any leading bits); and it has a single unambiguous code for zero. The all-zeroes negative full-scale code (0000), though not used in computing (because  $-F.S. + 1 \text{ LSB}$  is the most negative value defined in computing), is nevertheless useful as a converter checking and adjustment code.

The principal drawback of offset binary—unless the device is a sign-magnitude converter with translated logic—is that a major bit transition occurs at 0 (all bits change, from 0111 to 1000). This can lead to “glitch” problems dynamically (the difference in speed between bits turning on and off can lead to large spikes) and to linearity problems (the largest linearity errors are most likely to occur at major transitions, because the transition is essentially a difference between two large numbers). In offset binary, zero errors may be greater than with sign-magnitude, because the zero analog level is usually obtained by taking a difference between the MSB ( $\frac{1}{2}$  full range) and a bipolar offset ( $\frac{1}{2}$  full range)—again, two large numbers.

*Twos complement*, for conversion purposes, consists of a binary code for positive magnitudes (0 sign bit), and the twos complement of each positive number to represent its negative. The twos complement is formed arithmetically by complementing the number and adding 1 LSB. For example, the twos complement of  $\frac{3}{8}$  (0011) would be its complement plus 1 LSB, or  $1100 + 0001 = 1101$ . If it were a right-justified number on an eight-bit bus (i.e., 0000 0011), its twos complement would be 1111 1101.

Twos complement is a useful code computationally because it can be thought of as a set of negative numbers. Therefore, addition can be used instead of subtraction. For example, to subtract  $\frac{3}{8}$  from  $\frac{4}{8}$ , add  $\frac{4}{8}$  to  $-\frac{3}{8}$ , or 0100 to 1101 (i.e., 0000 0100 to 1111 1101). The result is 0001 (0000 0001), disregarding the extra carry, or  $\frac{1}{8}$ .

If the twos complement code and the offset binary code are compared, it can be seen that the only difference between them is that the MSB of one is replaced by its complement in the other (Nature’s way of helping converter manufacturers and users). Since both a digit and its complement are available from most flip-flops, an offset-binary-coded converter may be used for twos complement, just by using the complement of the MSB at the output of an A/D converter or at the output of a D/A converter’s input register. And vice versa. Many converters are manufactured with both the MSB and its complement available.

Converters that produce (or respond to) twos complement directly have the same disadvantages as those coded for offset binary; the conversion process is generally identical. It is feasible (as noted earlier) to get improved analog performance by the use of a benign sign-magnitude conversion, with the external code translated to twos complement.



*Ones complement* is a common means of (or first step toward) representing negative numbers, because it is obtained arithmetically by simply complementing all of a number's digits. Thus, the ones complement of  $\frac{3}{8}$  (0011 or 0000 0011) is (1100 or 1111 1100). When a number is subtracted by adding its ones complement, the extra carry (that is disregarded in twos complement), if present, causes 1 LSB to be added to the total ("end-around carry.") Thus, subtracting  $\frac{3}{8}$  from  $\frac{4}{8}$ ,  $0100 + 1100 = 0000 + 0001 = 0001$  (or  $\frac{1}{8}$ ). Similarly,  $0000 0100 + 1111 1100 = 0000 0000 + 0000 0001 = 0000 0001$ . A ones complement code can be formed by complementing each positive value to obtain its corresponding negative value, including—alas—zero, which is then represented by two codes, 0000 and 1111.

Besides its ambiguous zero, a disadvantage of this code in conversion is that it is not as readily implemented as twos complement. If it is not converted to twos complement before a D/A conversion with a twos-complement converter, by adding a 1 LSB increment digitally when the MSB is 1 (indicating a negative number), then the easiest way to implement the conversion is by performing a twos complement conversion, and—if the MSB = 1—adding the *analog* value of 1 LSB. The extra analog bit—in concept—can be added simply and elegantly by resistively dividing the digital MSB logic level down to the LSB's analog value and summing this attenuated signal, but it will not be free of errors and noise.

### 7.3.2 CODE CONVERSION

Code conversion may be desirable, either after A/D conversion or before D/A conversion, in order to make it possible to use a converter that produces the best results at the lowest cost (or one that simply happens to be available). For this purpose, the matrix of Table 7.9 succinctly outlines the relationships among the codes. For right-justified buses wider than the digital word, "Complement MSB" includes leading bits.

### 7.3.3 OTHER BIPOLAR CODES

The list of bipolar codes mentioned above may seem exhaustive, but it does not fully reflect the ingenuity and diversity of the computer and converter industries. There are a number of variations in more-or-less widespread usage that should be mentioned here because they will inevitably be encountered. Fortunately, they are based on codes we have already discussed and may be easily described.

*Modified sign-magnitude:* This is a version of sign-magnitude in which the polarity indication (i.e., the MSB) is complemented (1 for positive, 0 for negative).

*Modified one's complement:* Like modified sign-magnitude, a version in which the MSB is complemented (1 for positive, 0 for negative).


To Convert From To ↓ 	Sign Magnitude	2's Complement	Offset Binary	1's Complement
Sign Magnitude	No Change	If MSB = 1, complement other bits, add 00 . . 01	Complement MSB If new MSB = 1, complement other bits, add 00 . . 01	If MSB = 1, complement other bits
2's Complement	If MSB = 1, complement other bits, add 00 . . 01	No Change	Complement MSB	If MSB = 1, add 00 . . 01
Offset Binary	Complement MSB If new MSB = 0 complement other bits, add 00 . . 01	Complement MSB	No Change	Complement MSB If new MSB = 0, add 00 . . 01
1's Complement	If MSB = 1, complement other bits	If MSB = 1, add 11 . . 11	Complement MSB If new MSB = 1, add 11 . . 11	No Change

Table 7.9 Relations among bipolar codes.

**Complementary everything:** All of the above-mentioned codes may be completely complemented to form complementary sign-magnitude, complementary offset binary, complementary two's complement, and complementary ones complement. (These are, as explained earlier in this chapter, “negative true” versions.) Such codes, although they make life a little more complex, are the preferred coding for some now-popular “industry-standard” converter types based on early monolithic switching hardware. Users of monolithic and hybrid converters without registers should be prepared to adjust their thinking (and especially their test equipment) to include the possible application of complementary codes.

For the sake of completeness, Table 7.10 lists the codes mentioned above, for 3-bits-plus-sign.

#### 7.3.4. ARBITRARY BIASING AND SCALING

The conversion relationships discussed so far have been either strictly one-sided (0 to full scale) or symmetrical ( $\pm$  full scale). The reason for this emphasis is that most commercially available converters are built that way—as general-purpose devices.

However, since the principal relationship between the analog variable and the digital number for linear converters is *proportionality*, the repertoire of codes corresponding to a given resolution may represent any portion of the analog voltage or current range.

Number	COMPLEMENTARY CODES					
	Modified Sign- Magnitude	Modified 1's Complement	Comp. Sign- Magnitude	Comp. Offset Binary	Comp. 2's Complement	Comp. 1's Complement
+7	1 1 1 1	1 1 1 1	1 0 0 0	0 0 0 0	1 0 0 0	1 0 0 0
+6	1 1 1 0	1 1 1 0	1 0 0 1	0 0 0 1	1 0 0 1	1 0 0 1
+5	1 1 0 1	1 1 0 1	1 0 1 0	0 0 1 0	1 0 1 0	1 0 1 0
+4	1 1 0 0	1 1 0 0	1 0 1 1	0 0 1 1	1 0 1 1	1 0 1 1
+3	1 0 1 1	1 0 1 1	1 1 0 0	0 1 0 0	1 1 0 0	1 1 0 0
+2	1 0 1 0	1 0 1 0	1 1 0 1	0 1 0 1	1 1 0 1	1 1 0 1
+1	1 0 0 1	1 0 0 1	1 1 1 0	0 1 1 0	1 1 1 0	1 1 1 0
0+	1 0 0 0	1 0 0 0	1 1 1 1	0 1 1 1	1 1 1 1	1 1 1 1
0-	0 0 0 0	0 1 1 1	0 1 1 1	0 1 1 1	1 1 1 1	0 0 0 0
-1	0 0 0 1	0 1 1 0	0 1 1 0	1 0 0 0	0 0 0 0	0 0 0 1
-2	0 0 1 0	0 1 0 1	0 1 0 1	1 0 0 1	0 0 0 1	0 0 1 0
-3	0 0 1 1	0 1 0 0	0 1 0 0	1 0 1 0	0 0 1 0	0 0 1 1
+4	0 1 0 0	0 0 1 1	0 0 1 1	1 0 1 1	0 0 1 1	0 1 0 0
-5	0 1 0 1	0 0 1 0	0 0 1 0	1 1 0 0	0 1 0 0	0 1 0 1
-6	0 1 1 0	0 0 0 1	0 0 0 1	1 1 0 1	0 1 0 1	0 1 1 0
-7	0 1 1 1	0 0 0 0	0 0 0 0	1 1 1 0	0 1 1 0	0 1 1 1
-8				1 1 1 1	0 1 1 1	

Table 7.10 Modified and complementary bipolar codes.

For example, to encode the industrial transmitter current range from 4 to 20 mA in binary, using a 500-ohm resistor and the 2-to-10-volt portion of the range of a 0-10V A/D converter, simply apply the voltage without any transformation. However, a more range-efficient alternative would be to offset the input by  $-2$  volts, amplify by 1.25, and apply the resulting 0-10V signal to the converter, thereby making use of the entire range of available codes and improving resolution by 25%. In a sense, the conversion relationship between the original input and the digital output is an *offset binary* code. The subsequent digital processing would take this transformation into account via the software.

Another sort of arbitrary scaling might result if the analog signal were proportional to a temperature range of (for example)  $0^{\circ}$  to  $70^{\circ}\text{C}$ , and one desired a direct readout of temperature on a “dumb” digital voltmeter. A typical approach might be to scale the voltage directly to the temperature numbers (e.g.,  $10^{\circ}/\text{V}$ ) and apply it to a DVM with a 10-volt scale, with the location of the decimal point re-interpreted. The DVM would then provide a readout from 0 V to 7.0 V scaled from 0 to 70 in *engineering units*.

### 7.3.5 DACs AS MULTIPLIERS AND ADCs AS DIVIDERS

As noted in Section 5.2, The D/A converter can be thought of as a digitally controlled potentiometer that produces an analog output (voltage or current) that is a normalized fraction of its “full scale” setting. The output voltage or

current depends on the reference value chosen to determine “full scale” output. If the reference may vary in response to an analog signal, the output is proportional to the product of the digital number and the variable analog input. The polarity of the product depends on both the analog signal polarity and the digital coding and conversion relationship.

Four-quadrant multiplication is available, if the D/A converter accepts reference signals of both positive and negative polarities and the conversion relationship is bipolar. A typical conversion relationship for a 4-quadrant multiplying DAC having 3-bit-plus-sign twos-complement coding is shown in Figure 7.8, interpreting the multiplying DAC as a digitally controlled variable-gain amplifier.

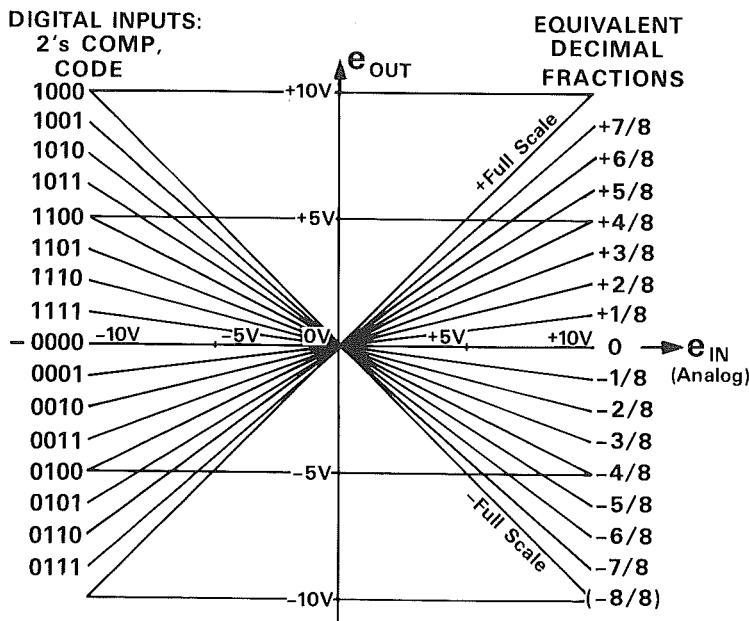


Figure 7.8. Digital-to-analog converter as four-quadrant multiplier of analog voltage and 3-bit-plus-sign, twos-complement digital number. Analog output vs. analog input as a function of digital input code.

In another interpretation, the envelope of the ideal bipolar D/A converter output in Figure 7.6 could be seen as proportional to the analog signal input, starting from full scale “Positive Reference,” being attenuated as the analog signal is reduced, passing through zero, and increasing negatively to the “Negative Reference” envelope.

When the input plane is viewed from above (digital number on one axis, analog input on the other—output along the axis of viewing), multiplying D/A converters may be 4-quadrant, two-quadrant (single polarity of either analog or digital variable), or one quadrant. In a sense, they may even be fractional-quadrant, if the reference or the code cannot be varied to or through zero.

In analog-to-digital converters, the digital output number depends on the ratio of the quantized input to the “full-scale” reference. If the reference is allowed to change in response to a second analog input, the digital output will be proportional to the ratio of the analog signal to the reference signal. Thus, the “ratiometric” A/D converter can be thought of as an analog divider with digital output. Generally, in such devices, the reference input has more limited range and dynamic capabilities than the signal input.

#### 7.4 ELECTRICAL INTERFACES WITH CONVERTERS

Converters may have associated with them six families of electrical inputs and outputs: analog signal(s), digital code, power, control, configuration, and reference. Table 7.11 indicates some of the properties of these interfaces, and the text that follows adds further detail.

	<b>D/A Converters</b>		<b>A/D Converters</b>	
<b>ANALOG SIGNAL</b>	Output:	Voltage or Current Polarity Magnitude	Input:	Usually Voltage Polarity Magnitude
<b>DIGITAL CODE</b>	Input:	Buffered or Direct Coding Logic Levels Format: Serial Parallel Byte-Serial	Output:	Coding Logic Levels Timing (Clock) Format: Serial Parallel Byte-Serial
	Output:	Readback		
<b>CONTROL</b>	Input	Strobe(s) Chip Select Chip Enable Write Reset	Inputs:	Convert Command Chip Select Enable Clock Chip
			Outputs:	Status Overrange
<b>CONFIGURATION</b>	Serial/Parallel Short Cycle ( ) Bits Address – Multiple On-Chip Devices		Byte-Enable Short Cycle ( ) Bits Address – Multiplexed Inputs	
<b>POWER</b>	Analog:	Usually $\pm 15V$ or same as Digital	Analog:	Usually $\pm 15V$ or same as Digital
	Digital:	+ 5V (TTL) + 5V to + 15V (CMOS)	Digital:	+ 5V (TTL) + 5V to + 15V (CMOS) – 5V to – 15V (CMOS $V_{ss}$ )
<b>REFERENCE</b>	Internal or External Fixed or Variable Polarity		Internal or External Fixed or Variable Polarity	

Table 7.11 Converter interfaces.

Figure 7.9 is a block diagram showing the relationships of typical connections to a parallel converter. There may be yet other connections, such as a clock synchronization input or output, complementary logic inputs or outputs, and

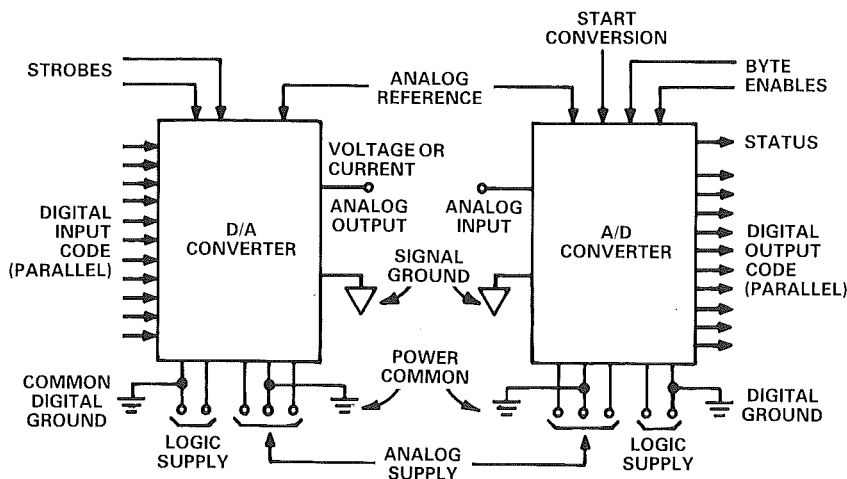


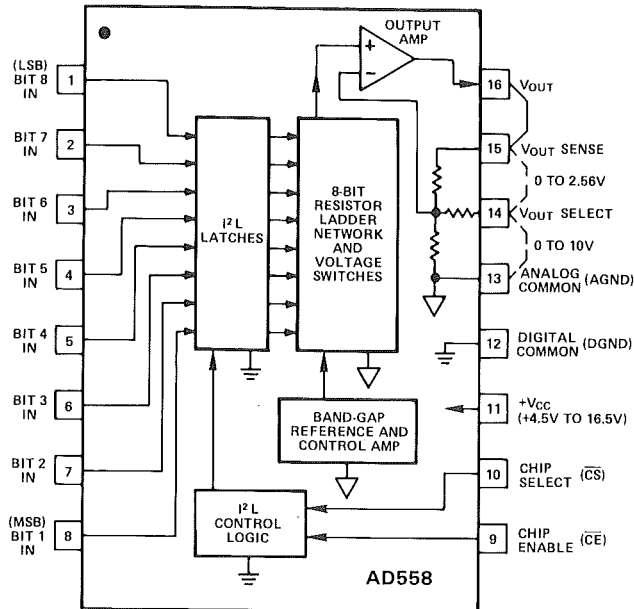
Figure 7.9. Typical classes of converter connection.

connections that are essentially internal but are brought out for the sake of optional flexibility, such as bipolar offset reference terminals. If the A/D converter is multiplexed, there will be additional analog inputs and one or more digital channel-select input lines. Figure 7.10(a) shows actual pin connections of a popular 8-bit IC DAC [AD558], and (b) shows the pin connections of a popular 12-bit IC A/D converter [AD574A].

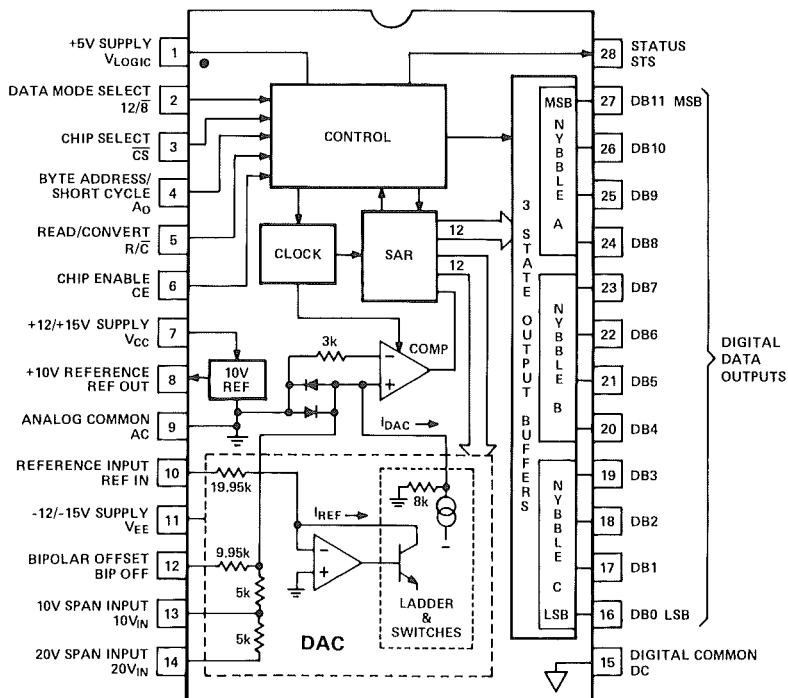
Application block diagrams in this book (and much of the literature), for facility of communication, tend to depict only those interfaces that are of specific relevance to the point under discussion. For example, when the logic interface is discussed, the analog aspect of the circuit may be ignored—and vice versa; in many cases, the power and ground connections are not shown in detail. However, the reader should be continually aware that “out of sight” must never mean “out of mind.”

#### 7.4.1 GROUND RULE

The experienced circuit designer will recognize the feeling of wariness provoked by the presence of two supplies, and several classes of signals, all needing return “to ground.” Grounding is indeed important to system performance; discussions of the essentials of grounding practice will be found (as appropriate) in several places in this book; however, for clarity in this present exposition, we will consider that all grounds are always at true zero potential with respect to all input and output signals. Accordingly, the discussions that follow will everywhere employ the inverted triangle, which represents ideal signal ground.



a. AD558 8-bit d/a converter (DACPORT™).



b. AD574A 12-bit a/d converter.

**Figure 7.10. Pin-connection schemes of actual devices.**

### 7.4.2 POWER SUPPLIES

The choice of power supplies for use with converters is governed by their effect on conversion accuracy, system noise, size and weight, reliability and cost. Supply capacity is determined by the choice of system philosophy: one main supply feeding all elements, vs. a number of satellite supplies or regulators sharing a common primary source (which might itself be a dc voltage derived from the ac mains). Generally, supplies that provide good operational-amplifier performance are sufficiently well regulated to provide rated converter performance, but adequate dynamic bypassing is essential because of the presence of fast digital edges. Converter performance as a function of dc variation of power supply voltage is a standard specification provided by the converter manufacturer. Conversion-system designers tend to avoid high-power switching-type supplies for converters.

### 7.4.3 DIGITAL LOGIC LEVELS

There are a variety of “standard” voltage levels and current-drive capacities corresponding to logic “0” and logic “1.” This variety is a result of historical compromises between circuit/processing technology, the need for speed, reliable differentiation between the logic states, circuit complexity, and fanout capability. They are described by such sets of initials as TTL, DTL, HTL, ECL, CMOS, IIL.

In general, logic levels are associated with device technology; the most popular of these are CMOS, ECL, and TTL. However, there are varieties of specifications and large variations within each family of devices; for example, low-voltage CMOS voltage levels are more closely related to TTL than to high-voltage CMOS. In fact, most of the modern conversion system products are designed for some degree of compatibility with TTL, the most widely used logic system.

Logic levels are closely related to supply voltage; in fact, the ideal logic gate would switch between ground and supply voltage, but voltage drops in the devices and in the external circuits require specification of logic 1 as somewhat less than supply voltage and logic 0 as somewhat greater than ground. TTL and low-voltage CMOS are based on widely used single +5-volt supplies.

In classical TTL, as mentioned earlier, a gate must respond to “0” if the input to it is 0.8 volts or less, and it must respond to “1” if the input is 2.0 volts or greater, up to the maximum and minimum voltage ratings. In order to provide a measure of immunity to noise, including dc voltage drops, occurring in transmission, gate outputs (within their current ratings), must furnish a minimum of 2.4 volts to signify “1” and a maximum of 0.4 volts to signify “0.”

Within the TTL system, there are further classifications by fanout (the number of gates that can be driven) and speed. For convenience, input or out-



put currents are normalized in terms of the standard *TTL load*, which is a positive current of  $40\mu\text{A}$  for “1” and  $-1.6\text{mA}$  (sink current) for “0”; however, an inspection of a random variety of “TTL-compatible” converter types (or even digital bit currents vs. digital control currents within the same converter) would often show substantial differences. To avoid possible difficulties at the interface, it is important for the user to read the manufacturer’s data sheet and understand what “TTL-compatible” means for a given device.

When CMOS devices operate at higher voltages, they usually (but not always) have increased noise immunity. CMOS devices in general draw low current except when switching; they have low power dissipation and accordingly higher circuit-packing density and are especially useful in remote and portable system elements.

Products designed for one logic scheme can be used with other logic schemes by performing appropriate transformations (level shifting, gain-or-attenuation, sign-inversion). D/A converters designed for TTL logic will inherently accept DTL Inputs.

#### 7.4.4 CONTROL LOGIC

##### *The Status Output*

In most applications, A/D Converters require a time interval, either fixed or variable, during which the system must wait for a conversion to be performed. During this time, the conversion data may be changing and may bear no relationship to the final result; if the input changes, it may cause erroneous results. Thus, the output of the converter must not be interrogated during the conversion, and the input track-hold must remain in the “hold” state until the input is ready to accept new data.

For this reason, the control output called *Status* (or “Busy,” “Data Ready,” “EOC”—*end of conversion*, etc.) changes state in response to the Convert command to define the conversion period; it does not return to its original state until a conversion is completed. It may be used as an interrupt, or to inhibit readout, or to update a *buffer* output register that holds the previous output word. It also serves to prevent another conversion from beginning, and to prevent the track/hold from changing state, until the converter’s input is ready. In some high-speed converters (for example, digitally corrected subranging types—see Chapter 13), and in tracking types, a new conversion may start as soon as the previous conversion has cleared the input stage and an earlier conversion has been latched into the output to activate the Data Ready line.

##### *Strobes*

Most D/A converters have basic circuitry that responds immediately and continuously to whatever digital signals are applied. It is often desirable to buffer the basic circuitry from the source of digital information (for example, a busy

bus) by a register, and update all bits simultaneously, upon command. The gating input is called the *strobe* (or “clock” or “enable.”)

For use with microprocessors, the data word is often divided into bytes, typically having 8 bits (see Chapter 4), or 4-bit *nybbles*; bytes are *enabled* in sequence to transmit the information contained in the full word in *byte-serial* format. Input strobes to DACs might be called *high-byte strobe* (more significant bits), *low-byte strobe* (less-significant bits), and—to load the complete information into the DAC—*load-DAC strobe* (often asserted at the same time as the final byte becomes valid). Conversely, the parallel outputs of ADCs are placed on the microprocessor data bus in appropriate order by *high-byte enable* and *low-byte enable* strobes. In order for the *status* output to be treated as information appearing on the data bus, a *status-enable* strobe would be used with microprocessor-compatible ADCs.

#### 7.4.5 ANALOG SIGNALS

Inputs to A/D converters are usually in the form of voltage. Outputs from D/A converters are often in the form of voltage, at low impedance, from an operational amplifier (an example is the AD667—Figure 8.8). However, many converters provide an active output *current* instead of a voltage (for example, AD567—Figure 8.6), and some simply provide an attenuation ratio; coupled with an op amp, they provide a digitally variable analog gain. As will become clear in the sections that follow, the basic conversion process may inherently develop a current output that is quite fast, linear, and free from offset. A built-in on-chip operational amplifier or an external op amp may be used to convert that current to voltage. As a result of the inevitable design tradeoffs, the amplifier will tend to limit converter performance, primarily by increasing settling time.

If the current is made available directly, the speed of response is under the control of the user, through the choice of an appropriate external output amplifier. The user can also choose the inverting or the noninverting mode. For example, in a 10-bit application calling for good accuracy and moderately high speed, at low cost, the full-scale settling time of the current output from the 10-bit AD561 to 0.05% ( $\frac{1}{2}$  LSB) is 250 nanoseconds. The AD561 (Figure 7.19), followed by a general-purpose I.C. operational amplifier for voltage output, typically has settling time of 5  $\mu$ s to the same resolution; but with a high-speed op amp, such as the AD509, for example, settling time can be reduced to 600ns.

Converters that have current outputs or “soft” voltage outputs (directly from resistive ladders) may be considered as either voltage generators with series resistance or current generators with parallel resistance (Figure 7.11).<sup>\*</sup> They are used with operational amplifiers in either the inverting or the noninverting

<sup>\*</sup>The impedance from summing point to ground is not always constant; a large class of converters—those using inverted ladders and connected directly to an op-amp summing point in the current-output mode—have code-dependent resistance and capacitance loading the summing point, affecting both linearity and dynamics.

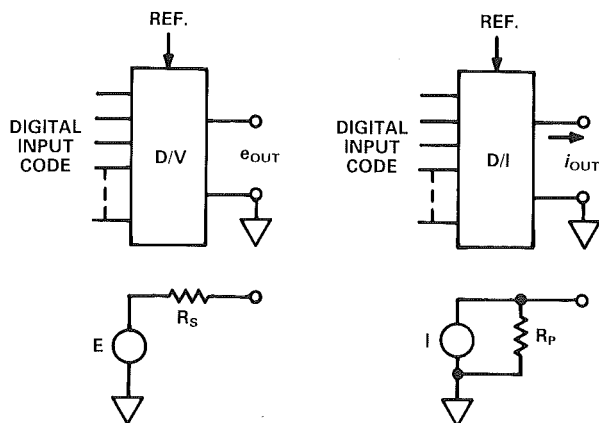


Figure 7.11. D/A converters as voltage or current generators.

connection (Figure 7.12). Some types have one or more internal feedback resistors (for appropriate output voltage scaling) that track the ladder resistors, to minimize temperature variations of gain in inverting configurations. Also present may be a terminating resistor, to develop passively a non-inverted output voltage, which may be amplified with a noninverting amplifier. The gain-determining feedback resistances ( $R_1$ ,  $R_2$ ) do not have to track the converter's internal resistors, only one another.

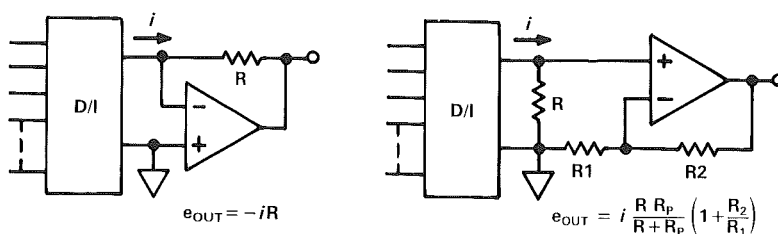


Figure 7.12. Current-to-voltage conversion, inverting and non-inverting, using operational amplifiers.

When current-output converters having active sources (see Figure 7.19 and Chapter 9) are used, the inverting connection is the preferred connection, for a number of reasons. With current-source output, the internal impedance of the D/I converter is usually high. Thus, the loop gain will tend to remain near unity, essentially independently of the value of feedback resistance, minimizing amplifier-contributed errors, such as voltage drift. Furthermore, the output swing of the D/I converter (at the amplifier's negative input terminal) will be negligible, minimizing loading of the current output—and any associated problems, such as voltage-dependent nonlinearity and variation of internal impedance with temperature. Finally, common-mode rejection is not important, since there is no common-mode swing.

However, if the DAC's basic circuit is that of a passively switched resistive attenuator (typical of CMOS DACs), a high-performance op amp must be used to minimize nonlinearity caused by voltage offsets and variable-impedance loading at the amplifier's summing point as codes are switched (see the next section and Chapter 12).

The conversion relationship of D/I converters is "positive reference" (Figure 7.6) if the current flowing *out of the converter* becomes more positive as the value represented by the digital code becomes more positive, irrespective of the actual polarity of the converter's reference element. If a noninverting amplifier configuration is used, the output voltage will have the same normalized conversion relationship as the output current. If an inverting connection is used, the voltage will have a conversion relationship of opposite output polarity, and will thus be "negative reference." Figure 7.13 illustrates this point, for both binary and complementary binary unipolar codes. On the other hand, if current flowing *towards the converter* increases as the value represented by the digital code increases, the relationship is "negative reference" for current, but "positive reference" for voltage in an inverting configuration.

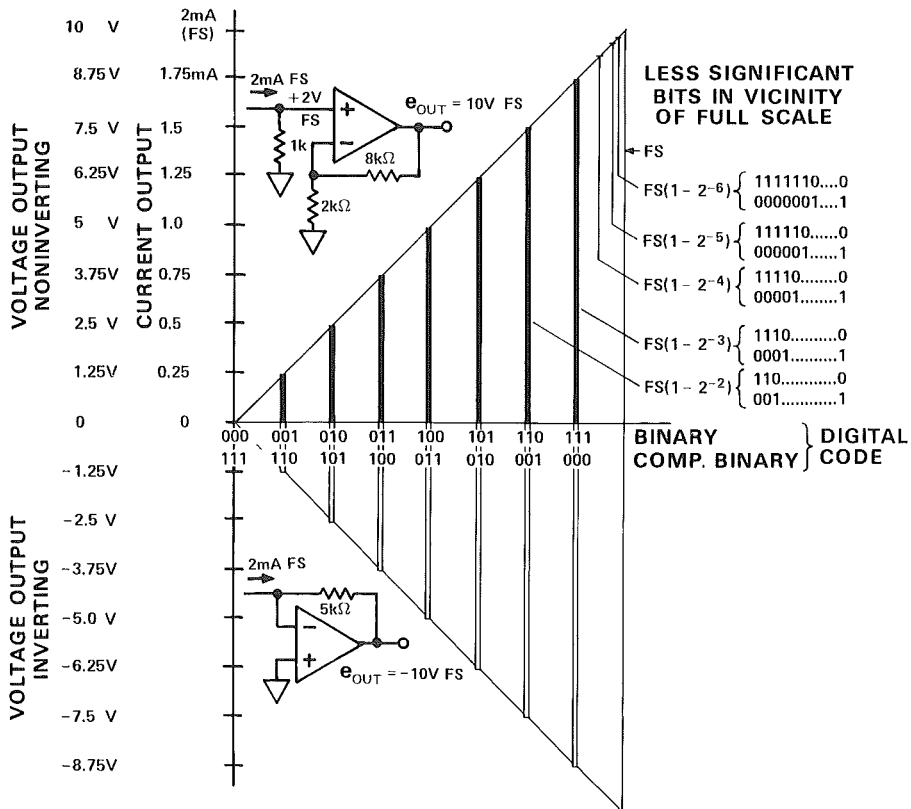


Figure 7.13. Ideal conversion relationships for the three most-significant bits in a positive-reference unipolar digital-to-current converter, with noninverting and inverting amplifier connections, and binary vs. complementary binary ("negative-true") codes.

## 7.5 D/A CONVERTER CIRCUITS

A basic D/A converter can be built with a voltage reference, a set of binary-weighted precision resistors, and a set of switches (Figure 7.14). An output buffer stage unloads passive elements, converts current to voltage or provides amplification, and furnishes a low-impedance voltage output.

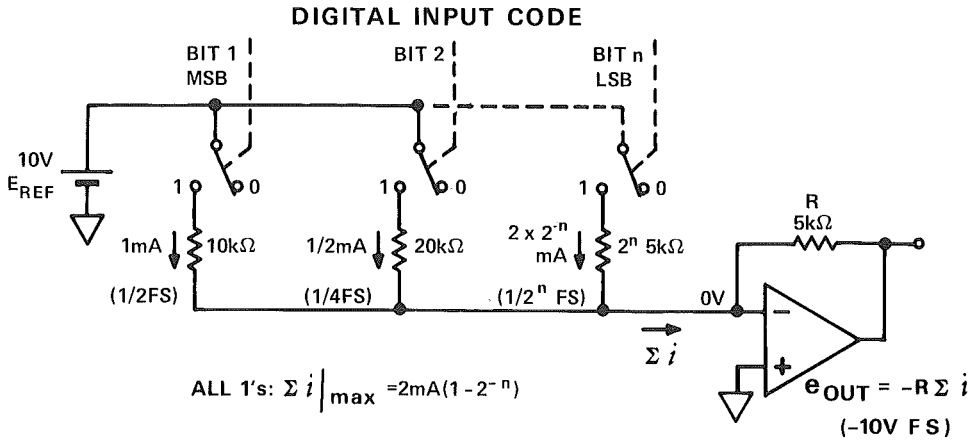


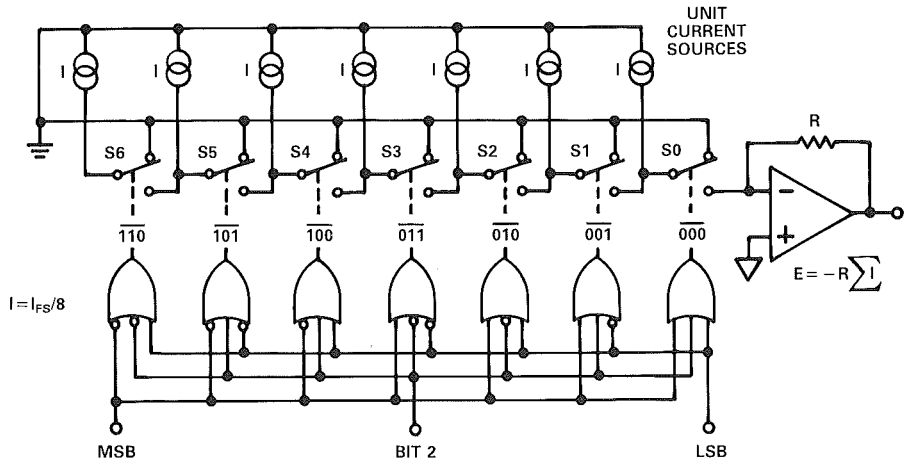
Figure 7.14. Simple digital-to-analog converter using binary-weighted resistors.

In this example, an operational amplifier holds one end of all the resistors in a set of  $n$  resistors at zero volts. The resistors are binary-weighted, i.e., each is weighted by  $2^j$ ; therefore, with equal voltage applied to all the resistors, the currents through them will be weighted by  $2^{-j}$ . The switches are operated by the digital logic, open for "0," closed for "1." Each switch that is closed adds a binary-weighted increment of current  $E_{\text{REF}}/R_j$  via the summing bus connected to the amplifier's negative input. The negative output voltage is proportional to the total current, and thus to the value of one of the  $2^n$  binary values represented by the input code. Thus, for an 8-bit converter and the code example of equation 7.2 (10111001), the output currents will be proportional to the terms in the equation, and the output voltage will therefore be proportional to the sum of the terms.

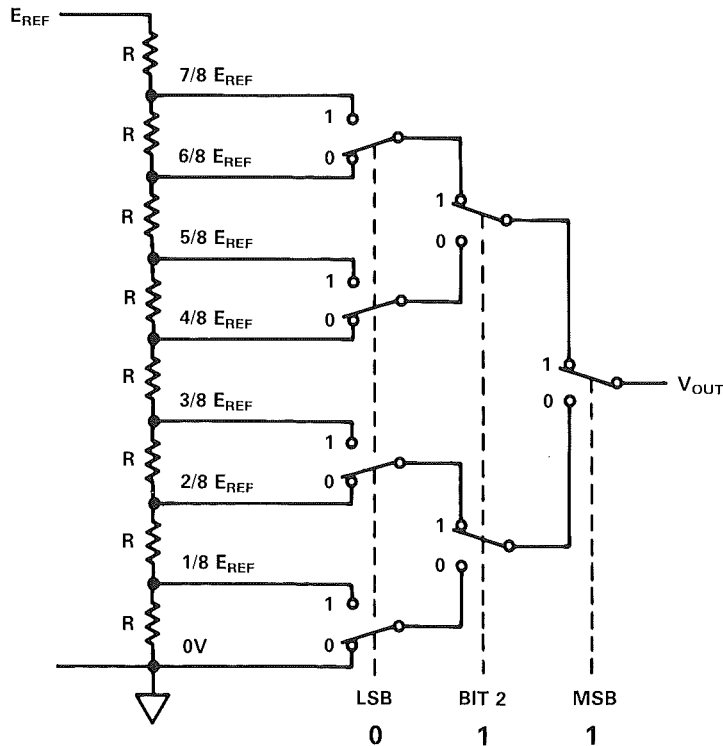
In general, for resolutions generally exceeding 4 bits, this scheme is not considered practical. For example, in 12-bit conversion, the required range of resistance values would be 2,048:1, or 20 megohms for the LSB to 10 kilohms for the MSB. If the resistors are to be manufactured in thin- or thick-film, or integrated-circuit form, such a range would be totally impractical. If discrete resistors are used, cost and size are increased, tracking advantages are lost, and inventory becomes a problem. Parasitic impedances (shunt and series) will also be difficult to deal with.

### 7.5.1 SWITCH DECODING

In the diagram of Figure 7.14, the selective summing of weighted currents provides the decoding. However, there is another approach, in which the binary code is digitally decoded, and  $N$  (from 0 to  $2^n - 1$ ) equal increments of current,  $I$ , are summed. Figure 15a shows an example of this technique for



a. Current-switching.



b. Voltage-switching.

Figure 7.15. Fully decoded 3-bit converter schemes.

3 bits, employing 7 equal current sources (or 7 equal resistors with a fixed reference voltage).

When all three bits are zero (000), switch  $S_0$  conducts its current to ground; no current flows through the op amp's feedback circuit. If one or more bits are 1,  $S_0$  will be closed, switching its current (as well as those from any other paths in a chain of consecutively closed switches) to the summing point. When the LSB only is 1 (i.e., 001), switch  $S_1$  will be open; for any other condition, it will be closed, allowing its source (etc.) to conduct toward the summing point—unless  $S_0$  is open. The position of any switch to the left of an open switch doesn't matter; its current flows to ground, not the summing point. Thus, corresponding to the binary chain of  $j$  codes, 000, 001, 010, etc., from 0 to 7, the sum of the currents flowing through the summing point will be  $jI$ . Figure 7.15b shows a corresponding scheme for a voltage-output DAC.

The principal advantage of fully decoded DAC architectures is that—assuming ideal switching—the output has to be monotonic, even if the resistor values or unit currents deviate substantially from their nominal values. Also, all resistors or current sources are identical. However, it is extremely difficult to carry out in practice, because  $2^n - 1$  resistors or current sources and switches are required, plus decoding logic and a great many interconnections.

Although these configurations have tended to be impractical for complete high-resolution DACs, a limited number of fully decoded bits are used in designs that combine them with another form of DAC architecture to simplify the problem of obtaining high resolution and monotonic behavior. Thus, for example, in a 16-bit D/A converter, the four-most-significant bits might use full decoding to divide the range into 16 equal parts, with an easier-to-build 12-bit converter providing the required 4,096 levels of interpolation in each portion of the range. Examples can be seen in the descriptions of devices in Chapter 8; typical high-resolution devices employing partial decoding include the AD6012 12-bit DAC, and the AD7546 and AD569 16-bit DACs.

### 7.5.2 RESISTANCE LADDERS

A way to reduce both the number of resistors and range of resistance is to use a limited number of repeated values, in a configuration providing suitable attenuation. One convenient approach, shown in Figure 7.16, is to use a binary resistance quad, consisting of four binary-scaled values (e.g.  $2R$ ,  $4R$ ,  $8R$ ,  $16R$ ) for each group of 4 bits, with attenuation of 16:1 for each successive quad, down to the least-significant quad. Thus, the four most-significant bits are summed without attenuation, the next four bits are attenuated by 16:1 and summed, and the last four bits are either attenuated by 256:1 and summed with the most-significant quad, or (more likely) attenuated by 16:1 and summed with the next more-significant quad. A benefit of this scheme is that the proper relative quad weighting for BCD conversion can be achieved by using the same scheme with an attenuation between quads of 10:1.

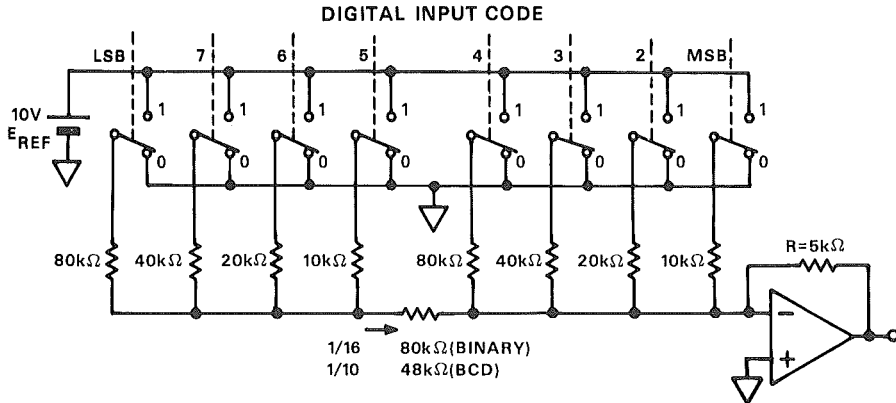


Figure 7.16. 8-bit digital-to-analog converter, using two equal-resistance quads with attenuation for the less-significant quad.

Carrying this reduction of resistance ratios farther, one arrives at the R-2R ladder, a convenient—and very popular—form. Figure 7.17 shows it with an inverting operational amplifier in a widely used configuration employing D/A converters that use CMOS switches.

If all bits but the MSB are “off” (i.e., grounded), the output voltage is  $(-R/2R) E_{REF}$ . For the second bit, the lumped resistance-to-ground of all the less-significant-bit circuitry (below the bit 2 leg) is  $2R$ ; the divider formed by series  $R$  and the two paralleled  $2R$  elements has an attenuation of  $1/2$ ; therefore,

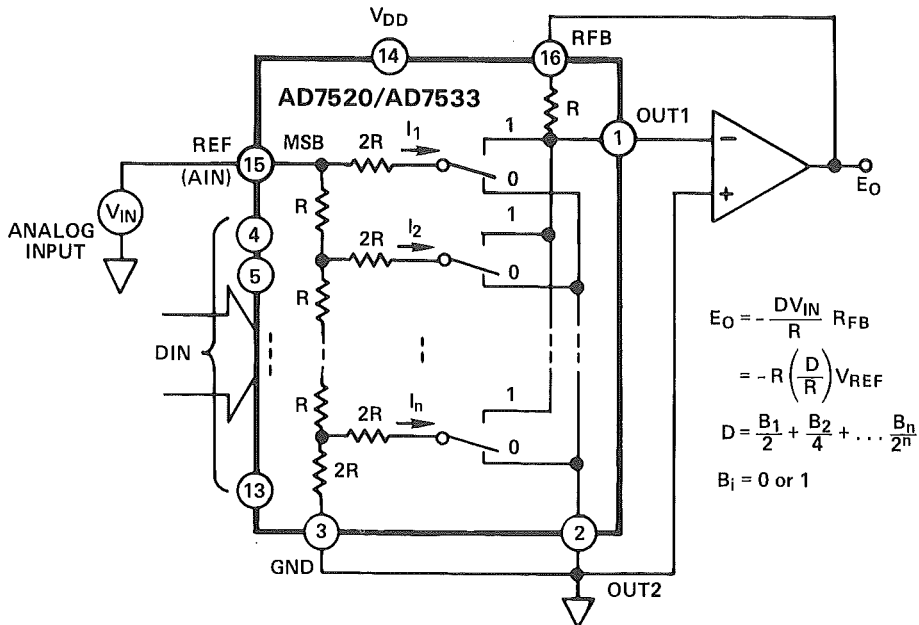


Figure 7.17. A typical CMOS DAC connected for conversion in current-steering mode. For clarity, not all resistance elements are shown.



if all bits but bit 2 are off, the current through the summing point will be one-half the MSB current, and the output will be  $(-1/2)(R/2R)E_{REF}$ . If Bit 2 is off, the same current will flow to ground. Continuing down the ladder, each  $2R$  resistor has one-half the voltage of the one above it, therefore it passes one-half the current. The output voltage is proportional (by superposition) to the sum of all the binary-weighted currents that have been switched on.

Because, in CMOS DACs, the switches are always very nearly at ground potential and will tolerate summing-point-type minuscule negative voltage swings, the reference can be either positive or negative, and the device can be used as digital gain control for ac signals or in four-quadrant multiplying DAC configurations.

The R-2R network can be employed to give unattenuated noninverting output *voltage*, simply by swapping the reference terminal and the output terminal. The reference terminal is driven at low impedance and the output terminal is connected to a high-impedance load, such as the input of a follower-connected operational amplifier (Figure 7.18). The effective resistance to ground of all resistors below a given node is  $2R$ . Therefore, if the MSB alone is on, the output will be  $(1/2) V_{REF}$ . When Bit 2 is on (all other bits grounded), its series  $2R$  and the lower  $2R$  form an effective generator of  $E_{REF}/2$  in series with  $R$ . Since that  $R$  is in series with another  $R$ , and an effectively grounded  $2R$  (via the MSB switch), the voltage at the output node is  $1/2$  the generator at node

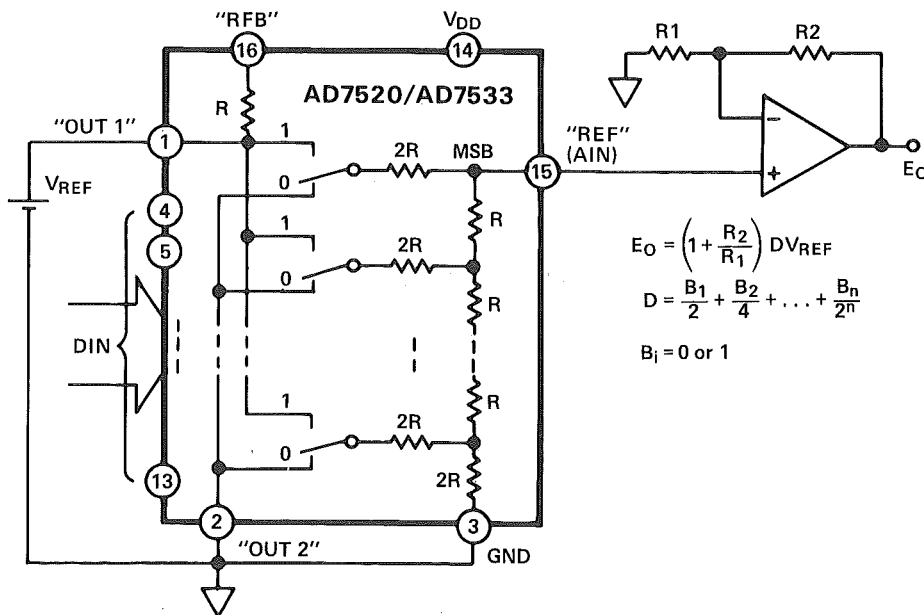


Figure 7.18. The same DAC as 7.17 connected for conversion in the voltage-switching mode. Generally, the magnitude of  $V_{REF}$  is limited in this configuration.

2, or  $(1/4) V_{REF}$ . The contributions of the subsequent bits form a binary progression, and superposition again provides an output proportional to the sum of the switched-on bits.

Since the entire network may be considered to be an equivalent generator having an output voltage  $D V_{REF}$  (where  $D$  is the fractional digital number), and an internal resistance,  $R$ , the output may be scaled down accurately by connecting precise resistance values to ground. Because of symmetry and self-duality R-2R networks may be used in other configurations. Some of these are discussed in Chapter 9.

### 7.5.3 SWITCHING

Needless to say, the switches used with the above networks are assumed here to be ideal. Switching may be performed in either the voltage mode or the current mode. A thorough description of the variety of voltage and current switches and switching schemes actually used in converters would be beyond the scope of this chapter. However, the use of monolithic bipolar transistor switches in converter design is addressed in Chapter 9. Information on popular converter designs will be found in Chapter 8, and a general discussion of CMOS switches will be found in Chapter 19. Considerable information about the characteristics of the switches used in CMOS DACs can be found in the *CMOS DAC Application Guide*, by Phil Burton, published by Analog Devices, Inc., 1985.

In the *current* mode, each leg of the ladder maintains constant current flow, which is steered either to an op-amp summing point or to ground. Two examples of current-mode converter block diagrams are shown in Figure 7.17 and 7.19. The first is that of a CMOS DAC, configured for current output. The bit currents are summed and converted to voltage via the feedback resistor, which is integrated on-chip, along with the ladder resistors, to maintain tracking of resistance with ambient temperature variations. This circuit is simple, and it can be used for 4-quadrant multiplication, but the presence of the switched resistors at the summing point of the op amp introduces problems with linearity in the presence of op-amp offsets, slowed dynamics due to switch capacitance, and noise coupling from the switch drive.

The second (Figure 7.19) is a DAC built on a bipolar chip. The design philosophy is described in some detail in Chapter 9. However, we can briefly describe here how it works: a buried Zener reference circuit develops  $-7.5$  volts, which is scaled by the inverting amplifier to  $+2.5V$ . Applied to amplifier A2, with its  $2.5\text{-k}\Omega$  input resistor, it causes a  $1\text{-mA}$  current to flow through the collector of reference transistor, Q1; the op amp adjusts the voltage across the  $5\text{-k}\Omega$  resistor to be whatever is necessary to maintain the feedback current at  $1\text{ mA}$ . Since the voltage applied to that resistor is also applied at the input of the R-2R ladder, we can expect that the currents in successive legs will have

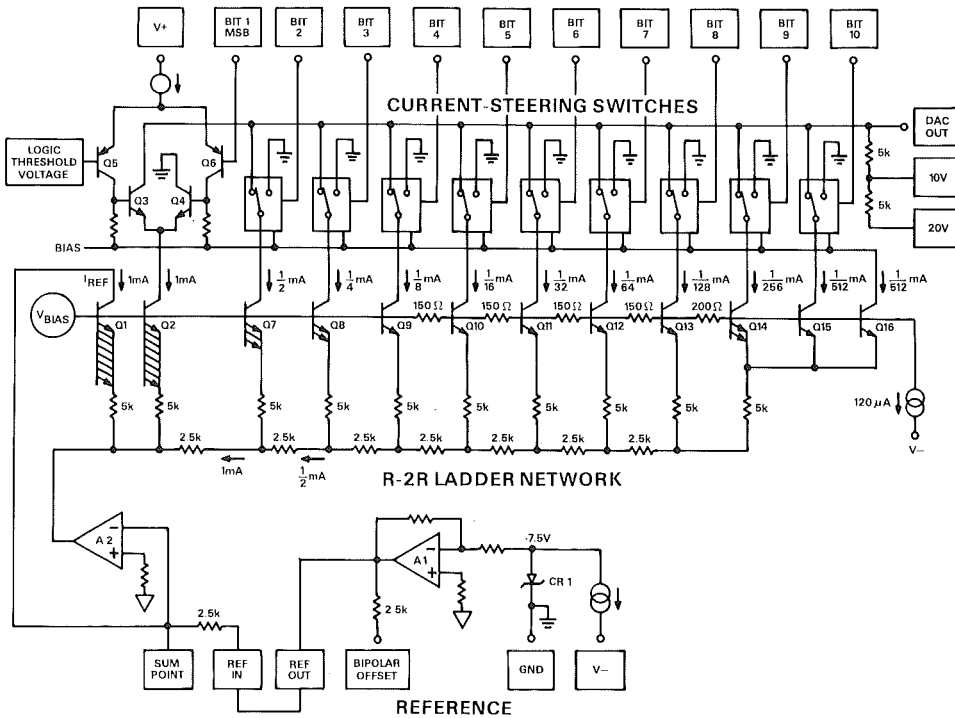


Figure 7.19. Schematic diagram of a current-output 10-bit DAC, showing reference, control amplifier, switching cell, and current-source arrangement.

a binary relationship; and, since Q1 is identical to Q2 (the MSB leg), the current that flows through its collector will also be 1 mA. The switches, which appear at the top of the diagram, switch the fixed currents either to ground or to the DAC OUT line, depending on the state of the control input for each bit.

While the reference in a DAC of this type is either fixed, or at best has a limited range of analog variation, the active reference circuit, compensated current sources, and fast-settling switches provide an excellent combination of speed and accuracy. A salient advantage of such current-mode converters is that the only significant voltage changes in the circuit appear at the output (in response to code changes); and the switch capacitances do not have to be charged through the ladder resistance.

Figure 7.18 shows a CMOS D/A converter being driven in the *voltage-switching* mode. In this mode, the ladder is used as a resistive attenuator; the switches alternate between a low-impedance reference voltage and ground. The magnitude of the current flowing through the switches is not important for precision, but the reference source and the switches must have sufficiently low impedance so that the current flowing through them does not cause significant voltage drops—or change in voltage drop as codes change.

For CMOS DACs in the voltage-switching mode, the constant resistance at the amplifier input (ladder output) eliminates linearity problems caused by modulation of the amplifier's offset voltage by code-dependent summing-point resistance in the current-steering mode of Figure 7.17. In addition, the switch capacitance is remote from the amplifier, and the charge is shunted to the input source or to ground, rather than to the summing point. Furthermore, the output capacitance of the network is considerably lower than in the current-switching mode. All of this results in cleaner and faster response of the circuit to code changes. As an additional feature, the system's output voltage is of the same polarity as the reference voltage; this makes it possible to operate the *DAC and its amplifier* from a single-polarity supply. Finally, only a single amplifier is required for bipolar digital operation, using offset binary or twos-complement coding.

The configuration has a few minor disadvantages. Performance is satisfactory for low values of reference voltage, but since the ON resistance of the FET switch is a function of the reference voltage, large values of reference voltage can produce significant nonlinearity. In addition, while current switching permits either polarity of input, only a single polarity of input is allowed in the voltage mode for CMOS DACs.

#### 7.5.4 REFERENCES

Reference circuits for connection to converters are discussed in some detail in Chapter 20. Still popular as a reference device is the temperature-compensated breakdown ("Zener") diode, often used with operational amplifiers for operating-point stabilization, unloading, or transducing to current (Figure 7.20). It is being supplanted for many new designs by band-gap references, ICs that act like synthetic high-performance Zener diodes, and Zeners on constant-temperature substrates. On integrated-circuit chips, reference voltages are provided by stable, quiet, buried-Zener references—laser-trimmed to minimize error and temperature coefficient—and by band-gap circuitry.

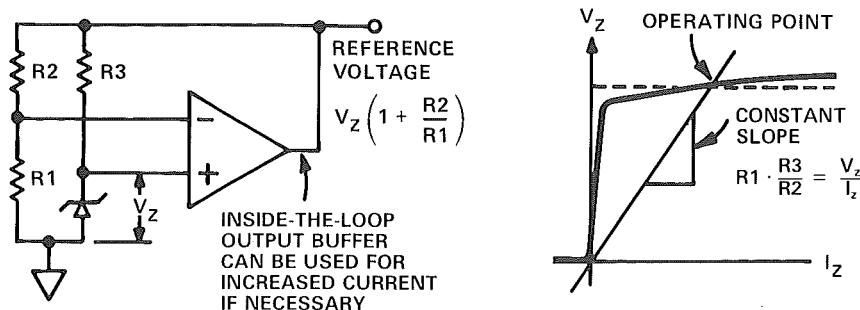


Figure 7.20. Stabilized diode reference. Amplifier adjusts feedback current to stabilize Zener-diode operating point independently of  $V_S$  or load variations.

In DACs employing active current sources, a reference must be provided that compensates for the characteristics of the current sources and switches. A powerful (patented) technique is described briefly in connection with Figure 7.19, and in some detail in Chapter 9.

### 7.5.5 BIPOLAR CONVERSION

For bipolar current-switching D/A conversion, using offset binary or two's complement codes, an offset current equal and opposite to the MSB current is added to the converter output. This may be accomplished with a resistor and a separate offset reference. More usually, it is derived from the converter's basic reference, in order to minimize drift of the output zero with temperature. It is usually jumpered externally, but there are converters in which the bipolar connection is programmed digitally.

The gain of the output inverting amplifier must be doubled, in order to double the output range, e.g., from 0-10V to  $\pm 10$ V. As indicated earlier (Figure 7.6), zero output corresponds to offset-binary 1 0 0 . . . 0 0, or two's-complement 0 0 0 . . . 0 0.

Figure 7.21 shows an example of a current-switching converter connected for bipolar output. Note that, because the amplifier is connected for sign inversion, the overall conversion relationship is "negative reference," i.e., + F.S. for all 0's (offset binary),  $-F.S. (1 - \text{LSB})$  for all 1's.

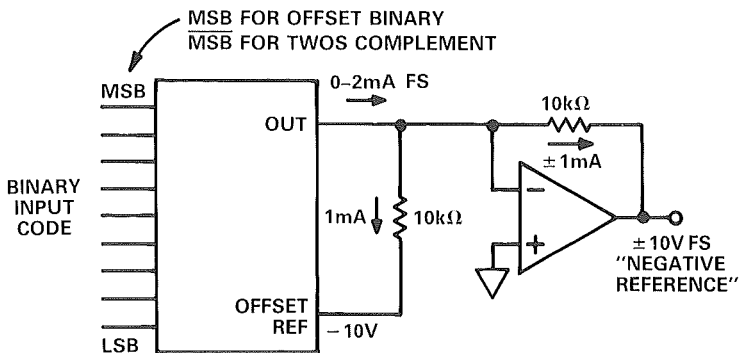


Figure 7.21. Bipolar connection of current-switching d/a converter for offset-binary or two's-complement codes.

For non-inverting applications, employing the output current of an active-current-source DAC to develop a bipolar output voltage across load resistance, the same values of offset voltage and resistance are used, but—for a given range of compliance voltage—the proper value of output voltage scale factor depends on the load presented by the parallel combination of the internal resistance, the offset resistance, the external load, and the gain of the buffering op amp. (Figure 7.22)

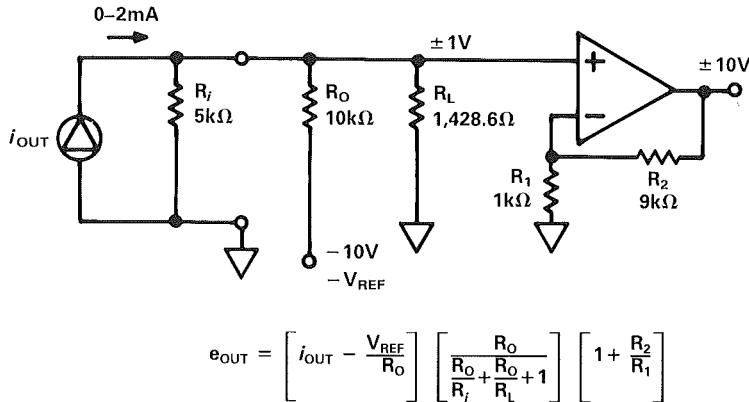


Figure 7.22. Non-inverting bipolar output from current-switching d/a converter.

For bipolar D/A conversion using CMOS d/a converters in the voltage mode, the circuit of Figure 7.23 may be employed. It is similar to the circuit of Figure 7.18, but provides for subtracting the reference from the ladder output. If  $D$  is the digitally set DAC coefficient, the amplifier output is  $2 D V_{REF} - V_{REF}$ . For  $D = 1/2$ , the output is zero; if  $D = 0$ , the output is  $-V_{REF}$ , and if  $D$  is all-1's, the output is  $(1 - 2^{-(n-1)}) V_{REF}$ .

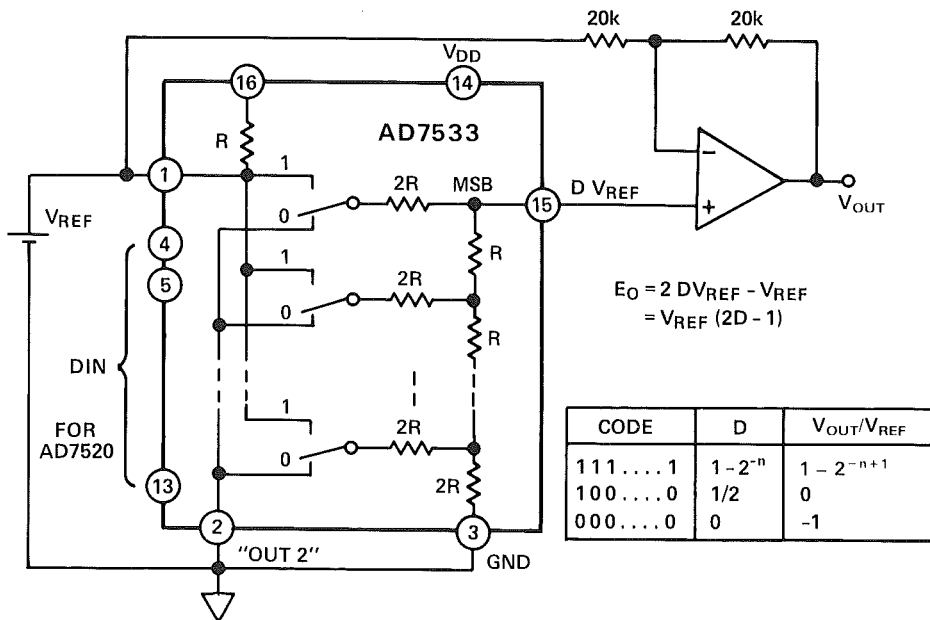
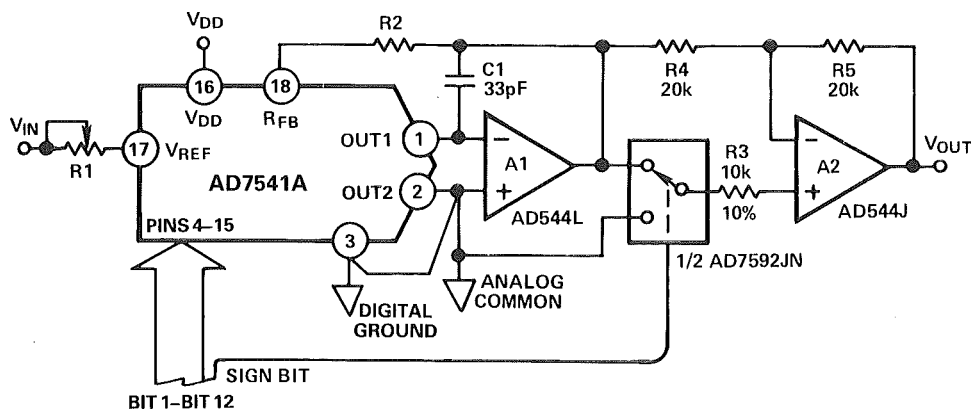


Figure 7.23. Connection of a CMOS DAC in the voltage-switching mode for bipolar operation. If  $V_{REF}$  is provided by a 2.5-volt source, such as the AD580, the nominal output swing is  $\pm 2.5V$ .





Sign Bit	Binary Number in DAC			Analog Output, $V_{OUT}$
	MSB		LSB	
0	1	1 1 1 1	1 1 1 1	$+V_{IN} \cdot \left( \frac{4095}{4096} \right)$
0	0	0 0 0 0	0 0 0 0	0 Volts
1	0	0 0 0 0	0 0 0 0	0 Volts
1	1	1 1 1 1	1 1 1 1	$-V_{IN} \cdot \left( \frac{4095}{4096} \right)$

Note: Sign bit of “0” connects R3 to GND.

Figure 7.25. Connecting a 12-bit CMOS DAC for sign-magnitude bipolar operation.

The basic parallel-input D/A converter circuits considered so far have the common property that the analog output continually tends to reflect the state of the logic inputs. However, if the basic conversion circuitry is preceded by a register, either external or internal, the DAC proper will respond only to the inputs stored in its register. When the register is latched, the analog output is unchanging. This property is universally required in bus-type data distribution systems, where data is continually appearing, but it is desired that a DAC respond only at certain times, then hold the analog output constant until the next update. In this sense, a DAC with buffer storage may be viewed as a sample-and-hold with digital input, analog output, and (conceivably) infinite “Hold” time.

The register is enabled by a *strobe*, the net gating signal that results, in microprocessor systems, when the specific device has been both addressed and given a *write* signal, which causes it to update. The limiting rate at which the strobe may be allowed to update is determined by two factors: the settling time of the DAC, and the response time of the logic. In general, settling time of the analog portion of the D/A converter is at least an order of magnitude



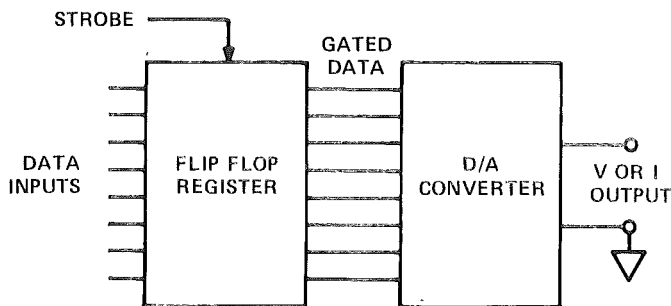


Figure 7.26. D/A Converter with buffer register.

slower than the response time of modern high-speed TTL logic circuits and is thus the limiting factor on update rate.

On-chip DAC register architectures vary. For example, a DAC may be single- or double-buffered—one or two registers—and the input register may accept data in more than one byte, or nybble, depending on the width of the bus to which it is to be interfaced. These structures are discussed in several places, notably in Chapter 3 and Chapter 8. If there are multiple DACs in the same package, they are generally connected to a single bus, which is an extension of the external bus; internal chip logic determines the manner of selection and updating.

The speed of the digital portion of a D/A converter is of especial importance when the “glitch” caused by unequal turn-on and turn-off times is an important factor in the application. The digital inputs to a DAC come from digital logic circuits, which may exhibit *skew*, or unequal turn-on and turn-off times. Skew is inherent in the on-off nature of saturated logic, such as TTL; symmetry is much more nearly achieved in ECL, which is always in the active range. The analog switches used in DACs also exhibit skew; however, even if the switch circuitry is specifically designed to minimize skew, the additional skew of the digital logic will constitute an irreducible minimum. In applications where it is an important factor, glitch energy (or *impulse*) can be reduced by using logic that is faster than would be necessary just to drive the analog switches.

## 7.6 A/D CONVERTER CIRCUITS

There are a vast number of conceivable circuit designs for A/D converters.<sup>7</sup> There are a much more limited number of designs available on the market in small, modular form at low cost, specifically designed for incorporation as components of equipment. The most popular of these are:

<sup>7</sup>See *Electronic Analog/Digital Conversions*, by H. Schmid (Van Nostrand Reinhold, 1970), and more recently, *Data Conversion Integrated Circuits*, edited by Daniel J. Dooley (IEEE Press—Wiley, 1980)—for an encyclopedic panoply of A/D (and D/A) converter circuit designs.

Successive-approximation types  
Integration (single-, dual-, & quad-slope and v-to-f) types  
Counter and “servo” types  
Parallel and modified-parallel types

Each approach has characteristics that make it most useful for a specific class of applications, based on speed, accuracy, cost, size, versatility.

### 7.6.1 SUCCESSIVE APPROXIMATIONS

Successive-approximation A/D converters are quite widely used, especially for interfacing with computers, because they are capable of high resolution (to 16 bits), and high speed (to 1 MHz throughput rates). Conversion time is fixed and independent of the magnitude of the input voltage. Each conversion is unique and independent of the results of previous conversion, because the internal logic is cleared at the start of a conversion.

Modern IC converters, such as the monolithic AD574A 12-bit ADC, include 3-state data outputs and byte controls to facilitate interfacing with microprocessors. A “three-state” output has, in addition to the normal “1” and “0” states, when enabled, a not-enabled condition, in which the output is simply disconnected via an open voltage switch. This permits many device outputs to be connected to the same bus—only the device that is enabled (one at a time) can drive the bus. Since many processor data buses are only 8 bits wide, 10- or 12-bit data must often be communicated in two steps, one “byte” at a time.

The conversion technique consists of comparing the unknown input against a precise voltage or current generated by a D/A converter (Figure 7.26). The input of the D/A converter is the digital number at the A/D converter’s output. The conversion process is strikingly similar to a weighing process using a chemist’s balance, with a set of  $n$  binary weights (e.g.,  $\frac{1}{2}$  lb,  $\frac{1}{4}$  lb,  $\frac{1}{16}$  lb ( $= 1$  oz),  $\frac{1}{2}$  oz,  $\frac{1}{4}$  oz, etc., for unknowns up to 1 lb.)

After the conversion command is applied, and the converter has been cleared, the D/A converter’s MSB output ( $\frac{1}{2}$  full scale) is compared with the input. If the input is greater than the MSB, it remains ON (i.e., “1” in the output register), and the next bit ( $\frac{1}{4}$  FS) is tried. If the input is less than the MSB, it is turned OFF (i.e., “0” in the output register), and the next bit is tried. If the second bit doesn’t add enough weight to exceed the input, it is left ON (“1”), and the third bit is tried. If the second bit tips the scales too far, it is turned OFF (“0”), and the third bit is tried. The process continues in order of descending bit weight until the last bit has been tried. The process completed, the *status* line changes state to indicate that the contents of the output register now constitute a valid conversion. The contents of the output register form a binary digital code corresponding to the input signal’s magnitude.

Figure 7.27a is a block diagram of a successive-approximations A/D conver-

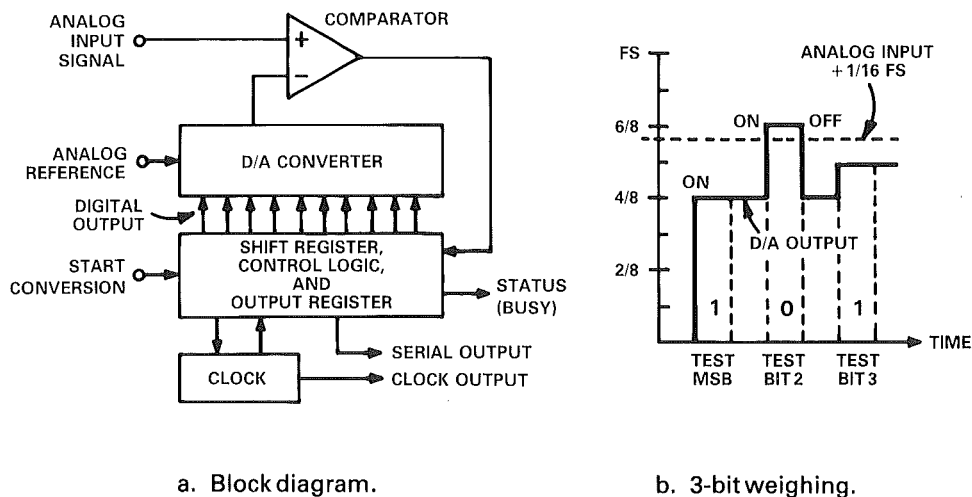


Figure 7.27. Successive-approximation a/d converter.

ter, accompanied by a time history of a simple 3-bit conversion, in terms of the D/A converter output (the weight added to the balance pan). Note that, to place the D/A converter output in the center of each ideal output quantum, a  $\frac{1}{2}$ -LSB “thumb” is placed on the scale (see Figure 7.2), in order to locate the transitions precisely at the  $\frac{1}{2}$  LSB points.

In the example of Figure 7.27b, the input does not change during conversion. If the input were to change during conversion, the output number could no longer accurately represent the analog input, for the same reason one would have difficulty using a chemist’s balance with a changing unknown. However, even if the final weight were to match the final unknown, there would still be a question as to whether the final unknown was itself legitimate, especially if the weighing had to occur at a specific time. To avoid any problems of this sort, it is usual to employ a sample-hold device ahead of the converter to retain the input value that was present at a given time before the conversion starts, and maintain it constant throughout the conversion. The *status* output of the converter could be used to release the sample-hold from its *hold* mode at the end of conversion. A sample-hold may not be needed if the signal (by itself, or with filtering) varies slowly enough and is sufficiently noise-free that significant changes will not be expected to occur during the conversion interval.

Accuracy, linearity, and speed are primarily affected by the properties of the D/A converter (and its reference), and the comparator. In general, the settling time of the D/A converter and the response time of the comparator are considerably slower than the switching time of the digital elements. The differential nonlinearity of the D/A converter will be reflected in the differential non-

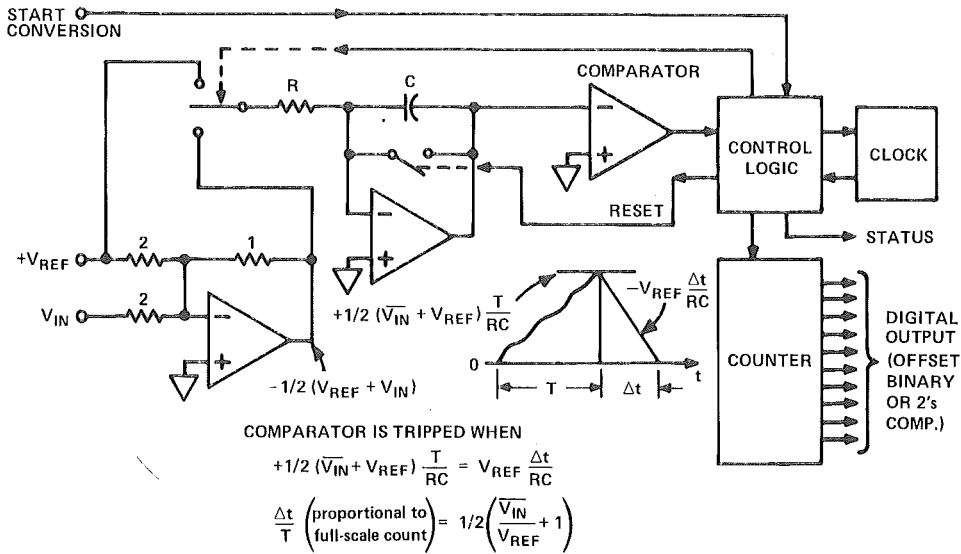
linearity of the resulting A/D converter. If the D/A converter is non-monotonic, one or more codes may be missing from the A/D converter's output range. Bipolar inputs are dealt with by using a D/A converter with bipolar output and offset binary coding, and appropriate input scaling.

### 7.6.2 INTEGRATION (RAMP AND V-TO-F TYPES)

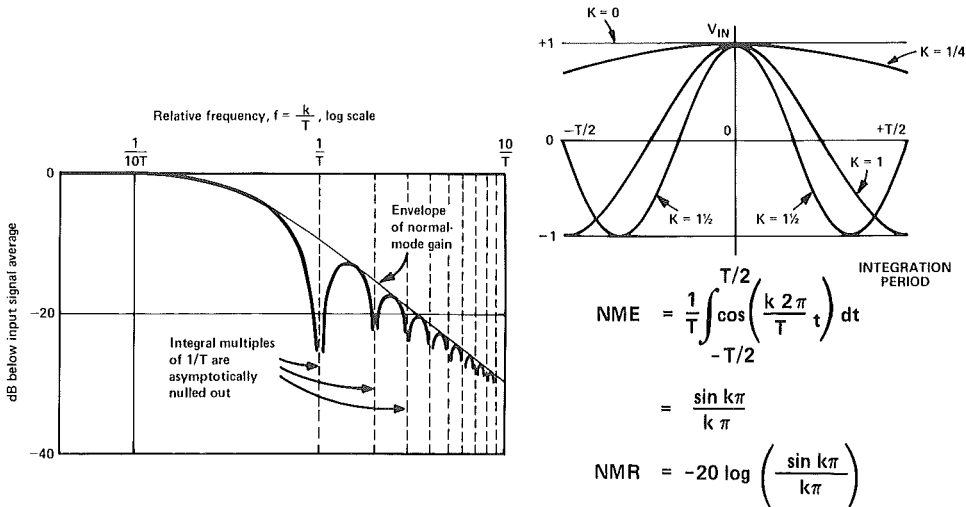
This family of converters is also quite popular. Its members perform an *indirect* conversion, by first converting to a function of time, then converting from the time function to a digital number using a counter. Integrating types such as the *dual-ramp* and quad-slope types are especially suitable for use in digital voltmeters and those applications in which a relatively lengthy time may be taken for conversion to obtain the benefits of noise reduction through signal averaging.

Here's how the dual-ramp type works: The input signal is applied to an integrator; at the same time a counter is started, counting clock pulses. After a predetermined number of counts (a fixed interval of time,  $T$ ), a reference voltage having opposite polarity is applied to the integrator. At that instant, the accumulated charge on the integrating capacitor is proportional to the average value of the input over the interval  $T$ . The integral of the reference is an opposite-going ramp having a slope  $V_{\text{REF}}/RC$ . At the same time, the counter is again counting from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to  $\overline{V_{\text{IN}}} T$ , and the equal amount of charge lost is proportional to  $V_{\text{REF}} \Delta t$ , then the number of counts relative to the full count is proportional to  $\Delta t/T$ , or  $V_{\text{IN}}/V_{\text{REF}}$ . If the output of the counter is a binary number, it will therefore be a binary representation of the input voltage. Converters of this type usually employ sign-magnitude coding for bipolar input ranges. However, if the input is attenuated and offset by half the reference voltage, the output will be an offset binary representation of a bipolar input, suitable as an input for computer systems (Figure 7.28a).

Dual-slope integration has many advantages. Conversion accuracy is independent of both the capacitance and the clock frequency, because they affect both the up-slope and the down-ramp in the same ratio. Differential linearity is excellent, because the analog function is free from discontinuities, the codes are generated by a clock and counter, and all codes can inherently exist. Resolution is limited only by analog resolution, rather than by differential nonlinearity; hence, the excellent fine structure may be represented by more bits than would be needed to maintain a given level of scale-factor accuracy. The integration provides rejection of high-frequency noise and averaging of changes that occur during the sampling period. The fixed averaging period also makes it possible to obtain "infinite" normal-mode rejection\* at frequencies that are integral multiples of  $1/T$  (see Figure 7.28b).



a. Conversion scheme for bipolar input.



b. Worst-case normal-mode response of dual-slope ADC.

Figure 7.28. Dual-ramp converter (voltage-to-time).

\*Normal-mode noise consists of unwanted signals that appear on the input line, even if common-mode error is nil. If a low-frequency or dc quantity is to be converted in the presence of a high-frequency ripple, a successive-approximations A/D converter, even if preceded by a sample-and-hold, will convert the instantaneous values of signal-plus-noise, producing a noisy digital signal. On the other hand, an integrator will inherently attenuate high frequencies, producing smoothing, and, if combined with a fixed averaging period, will null out those frequencies that have whole numbers of cycles during the averaging period.

Throughput rate of dual-slope converters is limited to somewhat less than  $1/(2T)$  conversions per second. The sample time,  $T$ , is determined by the fundamental frequency to be rejected. For example, if one wishes to reject 60Hz and its harmonics, the minimum integrating time is 16-2/3ms, and the maximum number of conversions is somewhat less than 30/s. Though too slow for fast data acquisition, dual-slope converters are generally quite adequate for such transducers as thermocouples; and they are the predominant circuit used in constructing digital voltmeters. Since DVM's use sign-magnitude BCD coding, bipolar operation requires polarity sensing and reference-polarity switching, rather than simple offsetting.

A shortcoming of conventional dual-slope converters is that errors at the input of the integrating amplifier or the comparator show up as errors in the digital word. Such errors are usually reduced by the introduction of a third portion of the cycle, during which a capacitor is charged with zero-drift errors, which are then introduced in the opposite sense during the integration, in order to (it is hoped) nullify them. An interesting scheme for nullifying most input errors is the patented *quad-slope\* principle*; it stores the errors in the form of a digital count during a calibration cycle and subtracts them from the final count during the conversion cycle.

Other conversion approaches in this class include the single-ramp type and v/f converters. In the single-ramp converter, a reference voltage, of opposite polarity to the signal, is integrated (while a counter counts clock pulses) until the output of the integrator is equal to the signal input. At that time ( $\Delta t$ ) the output of the integrator is  $E_{REF}\Delta t/RC$ . Therefore,  $\Delta t$ —hence, the number of counts and the corresponding digital number—is proportional to the ratio of the input to the reference. This process has the weakness that its accuracy depends on both the capacitor (extremely accurate and stable resistors are relatively easy to come by) and the clock frequency. In the v/f converter, a frequency is generated in proportion to the input signal; a counter measures the frequency and provides a digital output code, the value of which is proportional to the input signal. In both of the above schemes, offsetting may be used to obtain offset binary representation of bipolar analog inputs. V/F conversion is explored in some depth in Chapter 15.

### 7.6.3. COUNTER AND “SERVO” TYPES

Figure 7.29 is a block diagram of a counter-comparator A/D converter, which is analogous to the single-ramp type, but only conversion time (not accuracy) depends on the time scale. The analog input is compared with the output of a D/A converter, the digital input of which is driven by a counter. At the start of the conversion, the counter starts its count, which continues until the D/A

\*U.S. Patent 3,872,466

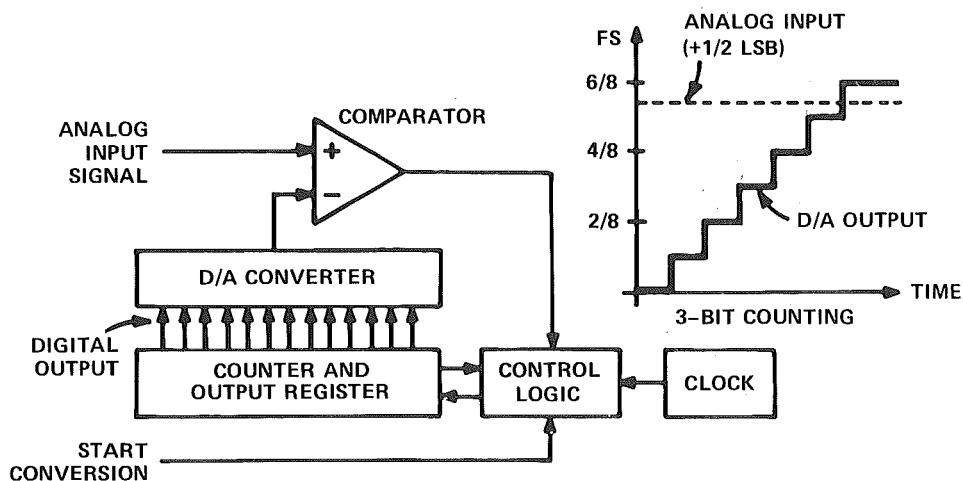


Figure 7.29. Counter-comparator a/d converter.

output crosses the input value. At that point, conversion ceases, and the converter is ready to perform the next conversion after the counter has been cleared and its output dumped into an output register. The number of counts appears in the output register. For bipolar inputs, a bipolar D/A converter is used, and the count is an offset binary representation of the input, starting from negative full-scale.

Though quite simple in concept, this converter has the disadvantage of limited speed for a given resolution, since the conversion time for a full-scale change is equal to the clock frequency divided into the maximum number of counts. For example, if the clock frequency is 10MHz, the maximum throughput rate for 10-bit resolution (1024 counts) is something less than 10kHz (100 $\mu$ s per conversion). A variation of this converter is the “servo” type, in which an “up-down” counter is used.

If the output of the D/A converter is less than the analog input, the counter counts up. If the D/A output is greater than the analog input, the counter counts down. If the analog input is constant, the counter output “hunts” back and forth between the two adjacent bit values. This “tracking” converter can follow small changes quite rapidly (it will follow 1 LSB changes at the clock rate), but it will require the full count to acquire full-scale step changes. The principle is widely used in resolver- and synchro-to-digital converters. Since it seeks to “home in” on the analog value, the analogy to a servomechanism is quite evident.

It seeks to convert continuously, which may be a disadvantage in tying it in with a fast data-acquisition system, since it can give a valid “conversion com-

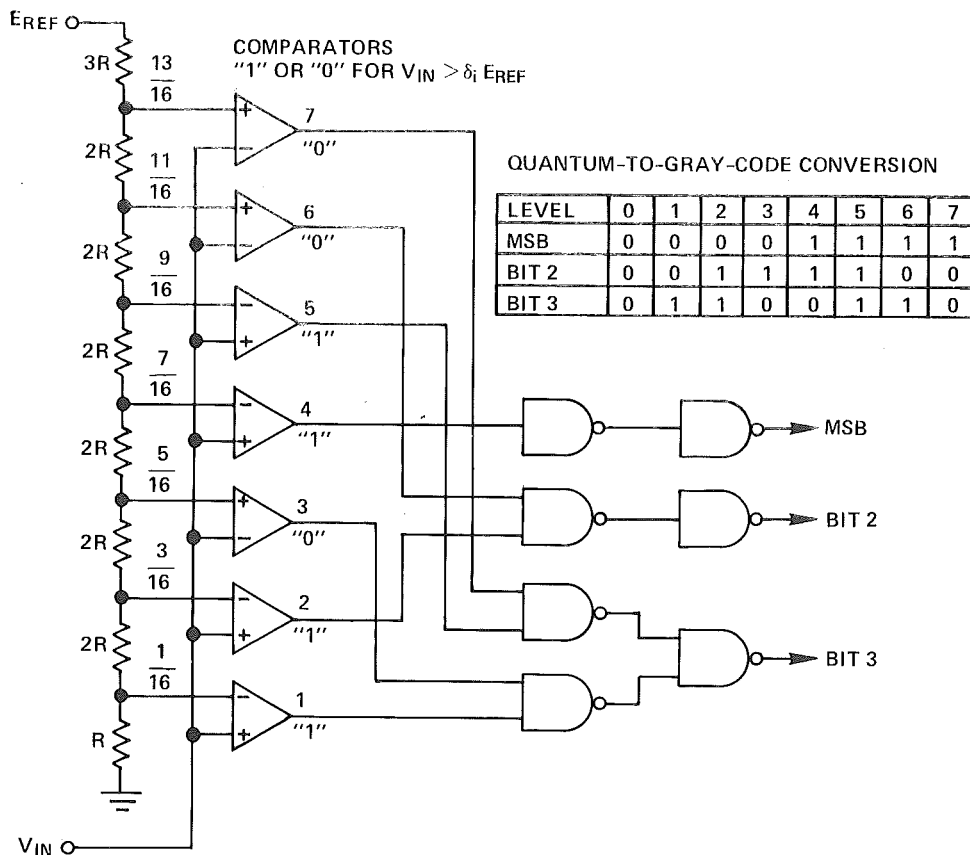


Figure 7.30. Parallel ("flash") 3-bit a/d converter with Gray-code output.

plete" report only during the clock period immediately following a change in state of the comparator (which in general occurs at irregular intervals). A buffer storage register may be used to store the previous count, while the counter is seeking the next value. By stopping the count (following a completed conversion) at an externally determined instant, the servo-type converter may be used as a sample-hold with arbitrarily long *hold* time (with no droop). If the "up" or the "down" count is disabled, the converter will act as a valley follower or a peak follower, counting in the appropriate direction only when the analog input exceeds the previous extreme value. Both the analog and the digital stored values are available.

#### 7.6.4 PARALLEL TYPES

Figure 7.30 shows a parallel 3-bit "flash" converter with Gray code output. It has  $2^n - 1$  comparators, biased 1 LSB apart, starting with  $+\frac{1}{2}$  LSB. For 0 input, all comparators are off. As the input increases, it causes an increasing



number of comparators to switch state. The outputs of the comparators are applied to the gates, which provide a set of outputs that fulfill the appropriate conditions for Gray-code output. (Natural binary could be implemented in the same way, using an appropriate table).

The evident advantage of this approach is that conversion occurs in parallel, with speed limited only by the switching time of the comparators and gates. As the input changes, the output code changes. Thus, this is the fastest approach to conversion.

Unfortunately, the number of elements increases geometrically with resolution. As linear and digital integrated-circuit elements of increasing complexity become available, increased levels of resolution will tend to approach the threshold of practicality. But high resolution and the fastest speeds at low cost are still some time away.

By combining parallel conversion for moderate numbers of bits with iteration (to wit, 6 or 7 bits of flash in two successive conversions, employing *digitally corrected subranging*—see Chapter 13), it is possible to strike a compromise that gives considerably better resolution than a parallel approach, with less complexity, and improved speed over the successive-approximation approach. For example, the CAV-1210 has 12-bit resolution at a rate of 10 megasamples per second.

#### 7.6.5 A NOTE ON SHARED LOGIC

In this book, we are concerned with the embodiment of the conversion function by means of ICs or other modules, in essentially complete form, with *completely defined specifications*. We should acknowledge, however, that when considering the tradeoffs between hardware and software, a software-oriented designer will be tempted to consider hardware savings inherent in using the control-logic capability of a microprocessor, along with basic precision analog functions (for example, a DAC with built-in reference and a precision comparator), to perform single or multiplexed conversions, employing the techniques mentioned here, but without using a piece of hardware identifiable as an “a/d converter” *per se*.

A decision to do this is in some respects equivalent to a decision to *design* a converter (analogous to the classical “make-or-buy” decision). It will tend to work well at low speeds and resolutions, in situations where the number of conversions required will not impose excessive time and software burdens on the processor. While there are applications for which the approach is eminently fruitful (e.g., dedicated instruments, to be manufactured in large quantity), the usual tradeoffs should be considered, lest the fascination of expending design- and manufacturing effort and software development in areas peripheral to one’s primary mission, lead one down the “primrose path” of wasted resources.

## *CONCLUSION*

In this chapter, we have attempted to provide the fundamentals for a basic understanding of converters. In the chapters that follow, we will discuss further some of the considerations faced and architectures employed by the converter designer, provide an understanding of and a guide to specifications of converters, and explore the elements of successful system design using converters.

# Chapter Eight

## Converter Microcircuits

This chapter endeavors to provide a thumbnail sketch of the wealth of integrated-circuit data converters available today, accompanied by historical insights into the technological influences affecting their development. Although no such summary from one source at one instant of time can be totally comprehensive or exhaustive, the reader should find the variety and diversity eminently satisfying.

### 8.1 INTEGRATED-CIRCUIT CONVERTERS

As the use of digital techniques in measurement, communication, and control grew by leaps and bounds, the size and price of processors and other LSI (and MSI) logic shrank in similar degree, with the inevitable result that further penetration of digital techniques into those fields became inevitable, in the regenerative fashion that is characteristic of the integrated-circuit era. Along with such other peripherals as keyboards, displays, and memories, converters have followed this spiralling trend—as a matter of necessity.

But it hasn't been easy. Linear IC's have always been more difficult to fabricate for reasonable degrees of resolution and accuracy than digital IC's—in part because the variables that are the input or output involve a continuum of voltage or current, rather than the easier-to-handle two-valued logic.

While the problems of implementing digital circuitry have involved questions of functions-per-chip, speed, and power dissipation, the analog (precision IC) problems have related more to simple existence and survival. Such matters as offset, bias current, drift, dynamic stability, common-mode errors, and open-loop gain—as well as slewing rate and settling time—have concerned both designers and users of op amps (the “representative” linear-IC product).

But converters are more difficult by at least an order-of-magnitude. While IC op amps called for precision transistor circuitry and clever design, and IC analog multipliers added a need for precision resistors (and references)—but to-date have attained accuracies to within 0.1% (at best) and are hardly in the commodity class—*converters* call for all of these prodigies of linear design and processing, and *more*: on-chip switches, logic, and everyday resolutions of up to 16 bits. Furthermore, the downward trend in price for digital functions carries over to the converter world, pressing converter technology to produce higher performance at lower cost.

Although the technology still has a considerable distance to go, it is worthwhile to consider the progress made, just within the past fourteen years, as measured by entries within the Analog Devices catalog. In the 1972 *Product Guide*, the IC conversion product line consisted of just two families of monolithic quad switches (and compatible resistor networks) for constructing precision 8-10-12-bit A/D and D/A converters.

In comparison, the 1984 Analog Devices *Integrated Circuits Databook* contains over 700 pages of data on converter microcircuits, including A/D, D/A, V/F, and S/D converters as well as a wide variety of support components, such as switches, multiplexers, references, and sample-hold amplifiers. Most of these products are monolithic.

Since monolithic technology has evolved to the point where low-cost data converters are readily available, many applications have become economically attractive in much the same way that the low-cost monolithic computer (microprocessor/microcomputer) made digital computation applications feasible. As microprocessors expand into more and more applications, analog input and output capability become increasingly important. The advances in monolithic converter technology have thus opened up vast new application areas.

### 8.1.1 PROCESSES

Converters have been manufactured using nearly all of the same monolithic processes used for fabricating digital devices. However, most digital processes are designed for highest possible speed and density, and lowest power, which often leads to small geometries and hence low breakdown voltages, limiting both power-supply and signal voltage ranges. While this is acceptable in digital circuits, it limits the dynamic range and resolution of data-converter circuits.

Modern microcircuit converters are manufactured with five generic technologies: bipolar, bipolar/ $I^2L$  (integrated injection logic), CMOS, BiMOS, and hybrid.

The *bipolar* process used for converters is fundamentally the same process used to manufacture classical linear functional devices, such as operational

amplifiers and voltage regulators. It has the advantages of being well-understood, due to its lengthy history, capability for high speed and low noise, and high breakdown voltages (leading to wide signal range). Its principal limitation is its generally poor logic capability, owing to the larger geometries used and relatively high power requirements.

*Bipolar/I<sup>2</sup>L* processing allows the standard process to include more complex logic functions, at the expense of slightly reduced breakdown voltages. Many data converters use this process, since it retains most of the advantages of traditional bipolar technology. It is interesting to note that the use of I<sup>2</sup>L is much more widespread in the data-converter world than in the digital world. This is because the speed-power product of MOS logic is more favorable than dedicated I<sup>2</sup>L. Thus I<sup>2</sup>L has evolved into a process with a specialized niche.

CMOS (Complementary Metal-Oxide Semiconductor) technology has evolved as the preferred MOS fabrication technology. It is superior to nearly all other processes in power requirements; and reduced-geometry devices are capable of speeds comparable to bipolar logic. In addition to these benefits, designers of data converters have found other advantages in CMOS. For example, one of the most common functions in data-converter designs is the analog switch. Switches can be produced in bipolar technology, but they are unidirectional, passing only currents of a single polarity. Bipolar transistors also exhibit a voltage drop (usually a junction—base-emitter—voltage) in series with the signal, and special circuit techniques must be employed in order to circumvent these shortcomings.

On the other hand, CMOS switches (also called transmission gates) have no  $V_{BE}$  drop to worry about. Since their switches act like resistors, they are also capable of passing current in either direction, which leads to the possibility of producing multiplying DACs that can operate with positive or negative, fixed or variable, reference sources. However, the limitation of the CMOS process that inhibits the use of CMOS for complete converters has been the lack of low-noise reference sources and gain (voltage-output) stages. Some operational amplifiers have been produced using CMOS technology, but they have fallen far short of the speed, stability, and low noise achievable with bipolar op amps. However, CMOS technology allows complex logic functions to be included on a converter chip, with very little additional power consumption.

*BiMOS* is a generic term applied to several manufacturing processes that combine bipolar and MOS transistors on one chip. This process is generally considered to be the most promising technology for future generations of data converters. It allows CMOS logic functions of low power and high density to be produced on the same chip as precision low-noise, high-gain, high-speed bipolar circuitry. Thus, it makes possible a complete converter with analog signal conditioning, conversion, memory, computation, and digital data communication—a “system-on-a-chip.”

*Hybrid* technology has been an effective method for the merging of multiple IC technologies in a single design—in order to produce a more complete function in a small package. Many have believed that, as monolithic technology progresses, hybrid technology must outlive its usefulness. However, quite the opposite is true. As monolithic technology has advanced, it has provided the hybrid designer with an increasingly large inventory of devices to choose from. Thus, hybrid technology will always have a place in converter manufacture, because it will always make possible higher performance and more complete functions in a single small package.

## 8.2 BIPOLAR D/A CONVERTERS

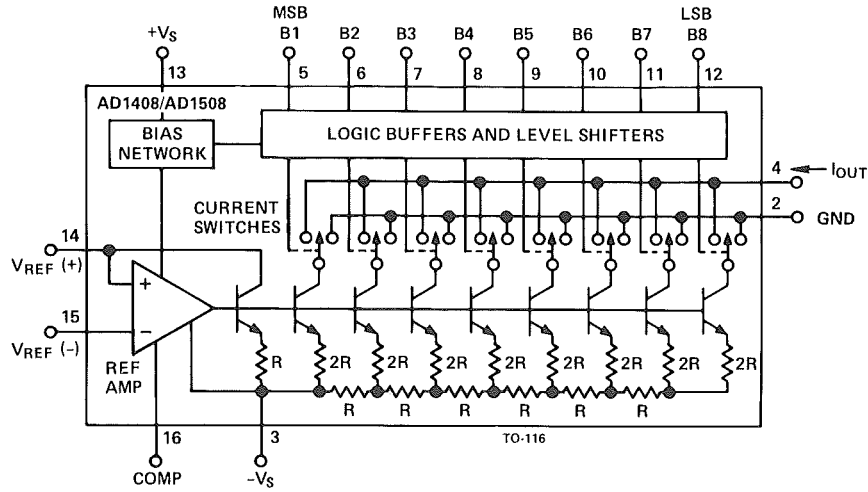
The earliest integrated circuit d/a converters were manufactured using bipolar technology; they included only the basic core of a complete DAC—the array of switches and resistors to set the weight of each bit (Figure 8.1a). The 1408 and a later, higher-speed derivative—known as the DAC-08—fall into this category.

These converters are produced by several manufacturers and are available at very low cost. However, they require many additional external components in order to be usable in a system design (Figure 8.1). These external components include several resistors, a reference, a latch, an output operational amplifier, possibly a compensation capacitor, and usually one or more trimming potentiometers.

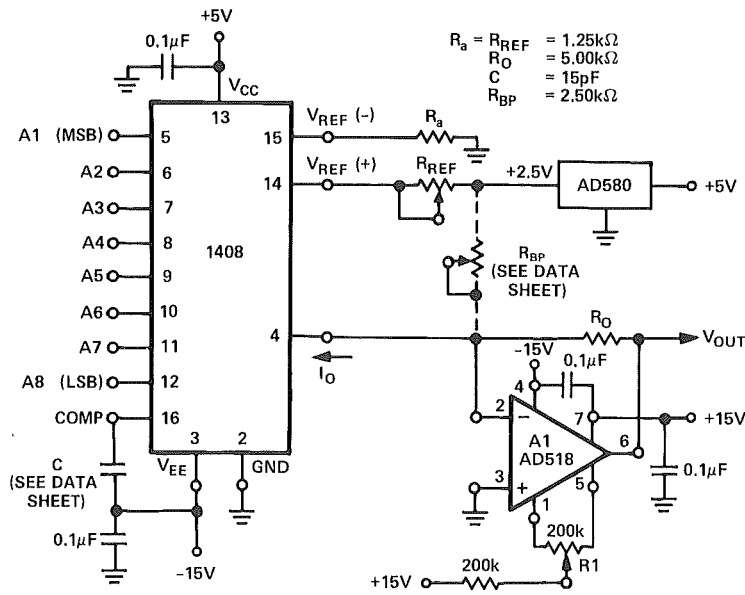
Converters like the 1408 were limited to 8-bit accuracy by the matching and tracking limitations of diffused resistors. The ability to match diffused resistors is limited by the definition of the resistor geometries in the photolithographic process, and post-fabrication adjustment is not possible. Furthermore, the temperature coefficient of diffused resistors is quite high, so that resistors which may match at room temperature could drift apart at other temperatures, causing degraded accuracy. When higher accuracy is desired, lower-tempco resistors are needed, and some means of post-fabrication adjustment is desirable.

Thin-film resistors exhibit low temperature coefficients and can be trimmed by use of a laser; they are well-suited for use in data converters. Thin-film resistors are manufactured using several different materials—silicon-chromium, nickel-chromium, and tantalum nitride are the most common. The resistor material is deposited on substates of ceramic, glass, or silicon, depending upon the manufacturer.

Hybrid converters have been manufactured with discrete switches and laser-trimmed thin-film resistor networks for quite some time. However, it was not possible to combine these components on a single monolithic chip (and thus produce a monolithic 12-bit DAC) until the late 1970s.



a. Functional block diagram.



$$V_{OUT} = \frac{V_{REF}}{R_{REF}} (R_O) \left[ \frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

ADJUST  $V_{REF}$ ,  $R_{REF}$  OR  $R_O$  SO THAT WITH ALL DIGITAL INPUTS AT LOGIC "1",  $V_{OUT} = 9.961$  VOLTS:

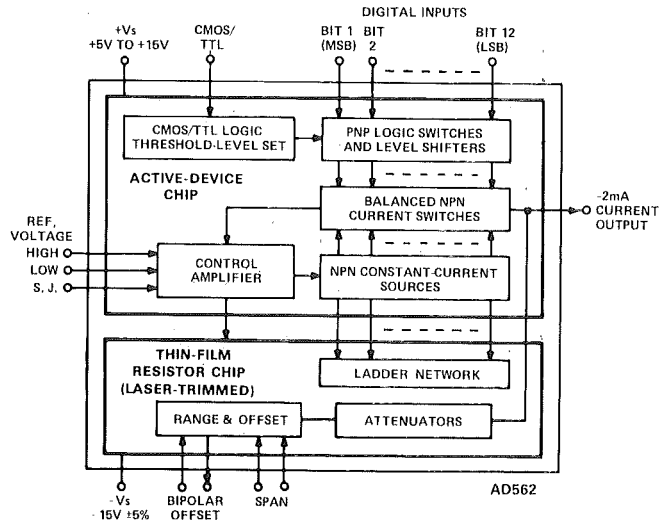
$$V_{OUT} = \frac{2.5}{1.25k\Omega} (5k\Omega) \left[ \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right] = 9.961 \text{ VOLTS}$$

b. Implementing a 1408 application (voltage output, fixed reference).

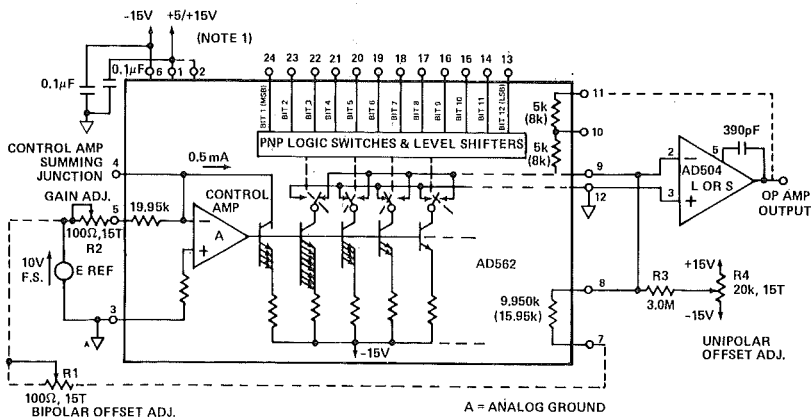
Figure 8.1. An early bipolar-process d/a converter design.

## 12-Bit DAC

The Analog Devices AD562 was originally manufactured using a variation of hybrid manufacturing known as “compound monolithic integration,” in which two IC chips were mounted in the same package without the traditional substrate for mounting and interconnection. Instead, the two chips were designed so that a set of wire bonds between the two chips (in addition to the usual ones to the package pins) were all that were necessary to assemble a 12-bit accurate DAC in an IC package.



a. Functional block diagram.



NOTE 1.

A. FOR TTL AND DTL COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND LEAVE PIN 2 OPEN.

B. FOR LOW VOLTAGE CMOS COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

C. FOR HIGH VOLTAGE CMOS COMPATIBILITY, CONNECT +15 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

NOTE 2. RESISTOR VALUES IN PARENTHESES ARE FOR BCD VERSION.

b. Functional schematic (recent version).

Figure 8.2. First 12-bit 2-chip DAC.



In the original AD562 (Figure 8.2), one chip contained the resistor network (including bit weight-setting resistors and output gain-setting resistors), and the other contained the reference control amplifier and the current switches for the 12 bits. As the processing matured, the manufacture of larger chips became more practical. The two chips of the original AD562 were merged into a single-chip version, which has since become available from other sources (multi-sourced); it became the first 12-bit DAC qualified by the U.S. Department of Defense under MIL-M-38510.

### Adding a Reference

While the AD562 was the first 12-bit IC DAC, and embodied the solution to some extremely difficult design problems, it was still really only a building block, since it lacked *latches*, a *reference*, and an *output amplifier*. Shortly after the two-chip AD562 was introduced, a version with a third chip was developed. The third chip was a 2.5-volt bandgap *reference*. This made the DAC function more complete. The resulting product, known as the AD563, also became quite popular and eventually made the transition to a monolithic device (Figure 8.3).

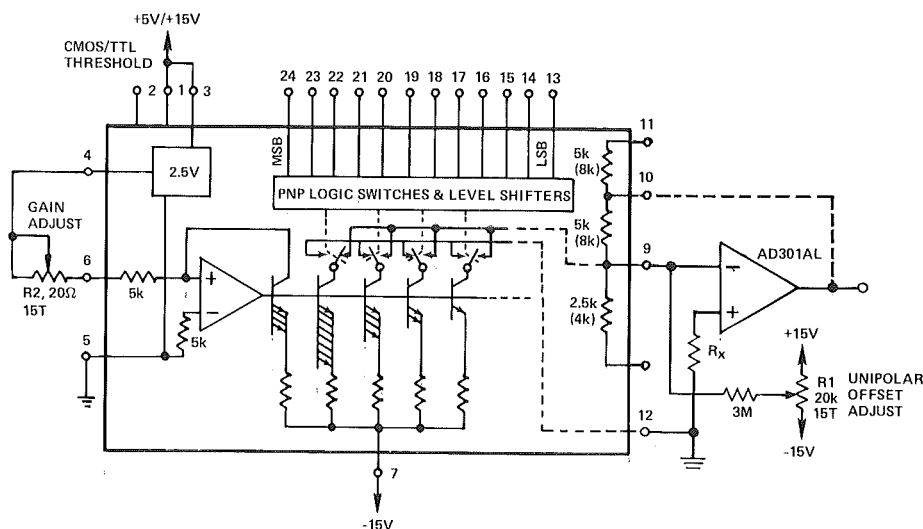
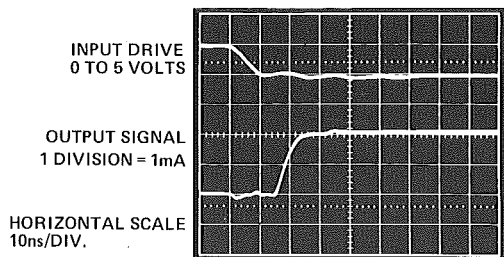


Figure 8.3. 12-bit bipolar-process DAC with additional 2.5-V reference.

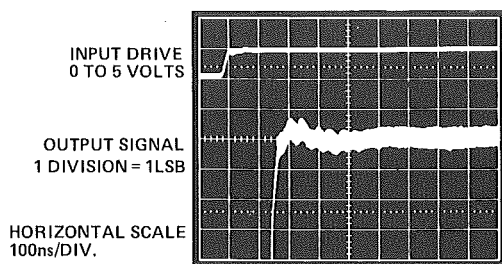
### Increasing the Speed

Another problem with the AD562 was that, while reasonably fast, it lacked sufficient speed for many applications; its settling time bordered on the slow side of the mystical 1-microsecond mark. Later advances in switch design and Zener-diode fabrication led to a higher-speed DAC, designated the AD565 (later followed by the AD565A). The bit switches used in this design are much smaller than those used in the AD562, allowing a substantial reduction in chip area and increasing the yield of good chips per wafer. The new switches also

operate faster, with a factor-of-five improvement in settling time (Figure 8.4), from 1 microsecond to 200 nanoseconds. Furthermore, the switches have an internal threshold for 5-volt logic compatibility, reducing power consumption and eliminating the need for a separate logic power supply.



a. Transition time; note 10-ns/division time scale.



b. Settling time.

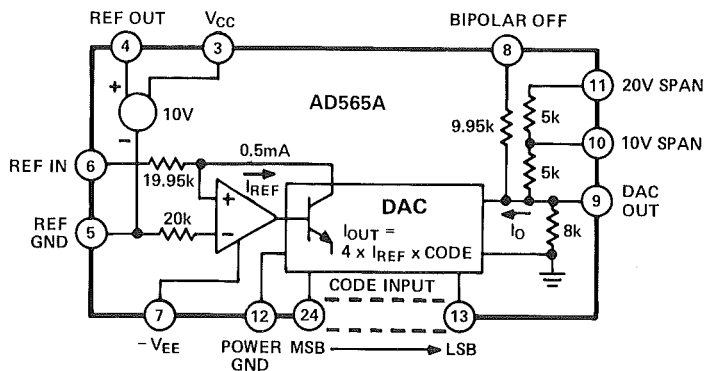
Figure 8.4. Full-scale transition and settling time of the AD565A.

Another improvement in the AD565 (Figure 8.5a) is the replacement of the bandgap reference by a buried-Zener type. The buried Zener differs from the conventional surface Zener in that the breakdown occurs below the surface of the chip. This frees the Zener from possible instabilities induced by migration of ions at the surface, as well as noise induced by imperfections at the silicon/passivation interface. The buried Zener also exhibits lower noise than the bandgap reference.

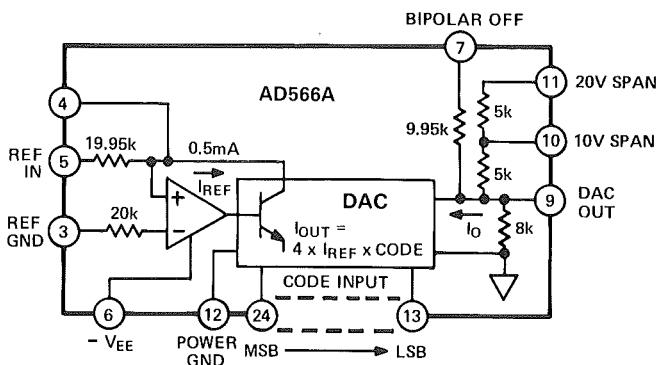
The AD565 retains the same pin configuration as the earlier AD563, allowing drop-in replacement in most applications with improved performance and lower price. An AD562-compatible version of the same chip is offered and is designated the AD566 (Figure 8.5b).

### *Adding Latches*

While these products offer 12-bit resolution and linearity, additional external components are necessary to apply them in systems. Specifically, *latches* are needed for the digital bus interface, and an *output amplifier* is needed to convert the output current to a more universal—hence more useful—output voltage, without the use of external precision components.



a. Complete version with reference (AD565A).



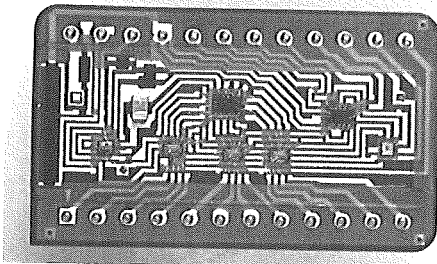
b. Speeded-up replacement for AD562 (AD566A).

Figure 8.5. Fast monolithic 12-bit bipolar-process DAC.

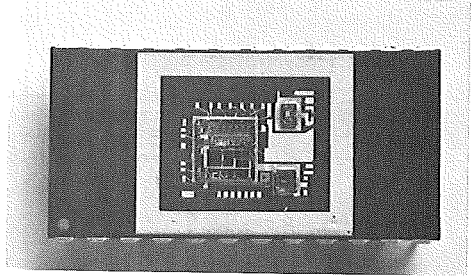
The evolution we are describing, towards the complete 12-bit bipolar DAC, progressed along two dimensions. The problem of adding the latches was solved in the AD567. This device is fundamentally similar to the AD565A, but includes latches implemented in an emitter-coupled logic form with TTL compatibility. These latches (Figure 8.6) are capable of accepting data in 4-bit nybbles, 8-bit bytes, or full 12-bit words from a bus.

The *double-buffered* arrangement of the latches allows the complete data word to be assembled in the first rank of registers, then transferred to the second rank, which drives the actual DAC inputs. This prevents invalid partial data (when using buses less than 12 bits wide) from reaching the DAC and generating spurious outputs during assembly of the complete data word. The latches are operated by independent address lines, gated with the Chip-Select and Write control inputs. The AD567 can operate with  $\overline{CS}$  and  $\overline{WR}$  pulses as short as 100 ns, and the current output settles to within  $\frac{1}{2}$  LSB in less than 500 ns.

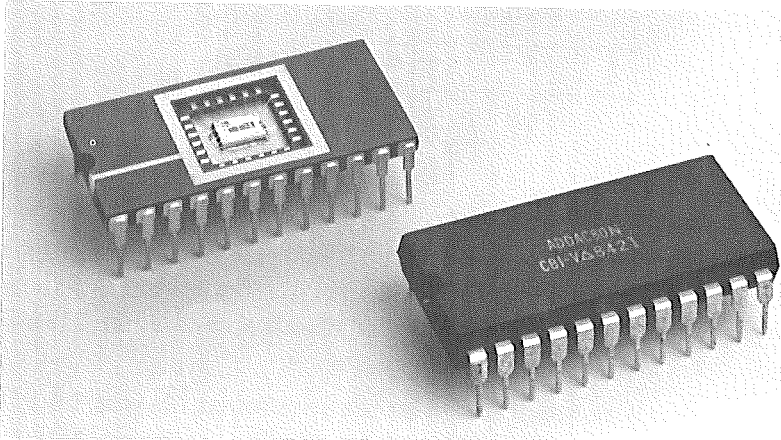




a. Early industry-standard version.



b. 3-chip version.



c. Completely monolithic version in ceramic and plastic packages.

Figure 8.7. Evolution of the DAC80.

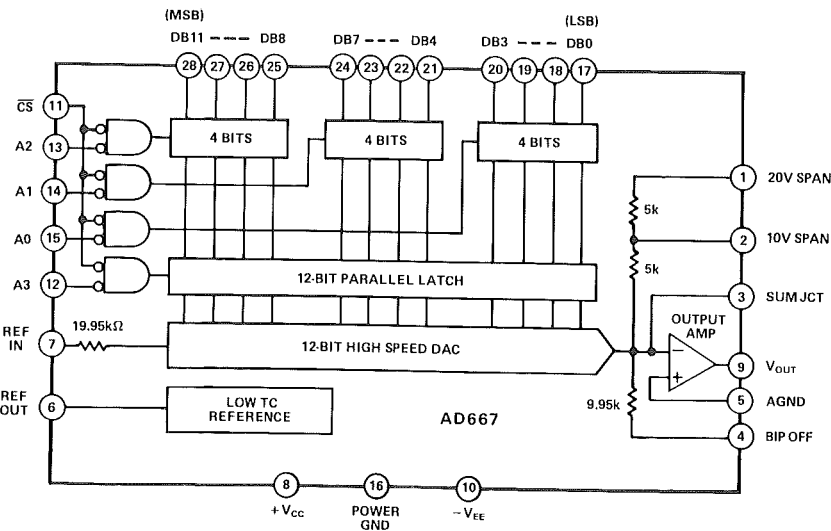


Figure 8.8. Functional block diagram of a complete, bus-compatible, voltage-output, monolithic 12-bit DAC.

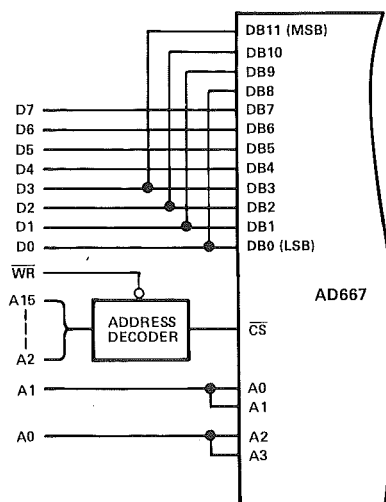


Figure 8.9. Connections of 12-bit DAC for right-justified interface to 8-bit bus.

chip bears a strong resemblance to the AD567, but includes the output amplifier that was used in the monolithic DAC80. Its applicability is enhanced by its availability in a variety of package forms: plastic and ceramic DIPs—and ceramic leadless chip carriers for surface mounting.

The AD667's positive-true digital data inputs are compatible with both TTL and 5-volt CMOS logic. Divided into 3 4-bit quads, they accept input data in a sequence of 4-bit nybbles from 4-bit buses; (8 + 4) or (4 + 8)-bit bytes (left- or right-justified—see Figure 8.9) from 8-bit buses; and 12 bits in parallel from 12- or 16-bit buses.

The inputs are double-buffered—this means that the converter may be updated when all 12 bits have been loaded, avoiding spurious analog output values. The control signals may be arranged for automatic updating when the full 12-bit word has been loaded. In addition, the double buffering makes it possible for a group of DACs to be updated simultaneously or in any desired sequence after having been loaded asynchronously by any of the above schemes. Since the latches are triggered by logic levels, rather than edges, they may be hard-wired in a transparent mode.

The on-chip 10-volt ( $\pm 1\%$ ) reference, which the user may externally jumper to the device input, with typically 1 mA to spare, may also serve other devices or as a system reference. The output voltage may be pin-programmed for bipolar outputs of  $\pm 2.5\text{V}$ ,  $\pm 5\text{V}$ , or  $\pm 10\text{V}$ , and unipolar outputs of  $+5\text{V}$  or  $+10\text{V}$ , at up to 5 milliamperes. A current booster may be connected inside the output op-amp's loop for high-current applications (e.g., line driving).

The use of precision high-speed bipolar current-steering switches and an on-chip high-speed output amplifier results in a  $10\text{ V}/\mu\text{s}$  slew rate and output-voltage settling time of  $3\mu\text{s}$  maximum to within  $\pm \frac{1}{2}$  LSB for a 10-volt change;

for 1-bit changes, typical settling time is  $1\mu\text{s}$ . The digital latch responds to strobe pulses as short as 100 nanoseconds, allowing the device to be used with fast microprocessors.

As an example of the specifications of a “universal” DAC, available in a number of performance options, all versions of the AD667 have guaranteed monotonic behavior over the specified temperature range. The AD667K ( $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ) and AD667B ( $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) guarantee maximum linearity error of  $\pm \frac{1}{4}$  LSB at  $+25^{\circ}\text{C}$  and maximum differential and integral linearity errors of  $\pm \frac{1}{2}$  LSB over temperature. Initial gain error is 0.2% of full scale (max) and offset is 2 LSB (max), while maximum temperature coefficients are  $\pm 15$  ppm of full-scale range per  $^{\circ}\text{C}$  for gain,  $\pm 3$  ppm/ $^{\circ}\text{C}$  for offset, and  $\pm 10$  ppm/ $^{\circ}\text{C}$  for bipolar offset.

### 8.2.1 COMPLETE 8-BIT DACS

Although the 12-bit DAC has arrived, it should not be forgotten that it once epitomized the goal of a supreme achievement in IC converter design, having the capability of resolving to 1 part in 4,096 and dealing in specifications expressible in tiny fractions of 1%, or even in parts per million. There are many applications that call for specifications that are far more modest in nature, easily satisfied by an 8-bit d/a converter capable of interfacing with an 8-bit bus, as long as it is complete, compact, low in cost, fast, easy to use, and of accuracy commensurate with its resolution.

The primitive 8-bit bipolar d/a converters mentioned earlier have historically been mere building blocks from which to build the DAC function. Devices like the 1408 and DAC-08 require many external digital and analog components, and adjustments, in order to perform what should be a relatively simple function. The need for a complete 8-bit DAC function was satisfied in 1980, with the introduction of the AD558 DACPORT<sup>TM</sup>, an 8-bit DAC which can be considered truly complete (Figure 8.10).

It contains a precision voltage reference, an output amplifier, a latching register with *nor*'d CHIP SELECT and CHIP ENABLE inputs, for efficient microprocessor interfacing, and a precision DAC circuit.

Laser-trimming at the wafer stage eliminates any need for external adjustments; all versions are monotonic over temperature, and calibration accuracy is guaranteed over the full temperature range to within  $\pm 1$  LSB at full scale or zero (“K” and “T” versions).

Truly microprocessor-compatible, the device will run from the same single supply used by the host microprocessor, at any voltage from  $+4.5\text{V}$  to  $16.5\text{V}$ , with a choice of two output ranges: 0 to  $2.56\text{V}$  ( $10\text{ mV/bit}$ ) and 0 to  $10\text{V}$  ( $39.1\text{ mV/bit}$ , for  $V_{\text{CC}} \geq 11.4\text{V}$ ). Settling time to full scale (Figure 8.11) is typically  $0.8\mu\text{s}$  to within  $\frac{1}{2}$  LSB ( $2.56\text{-V}$  range).

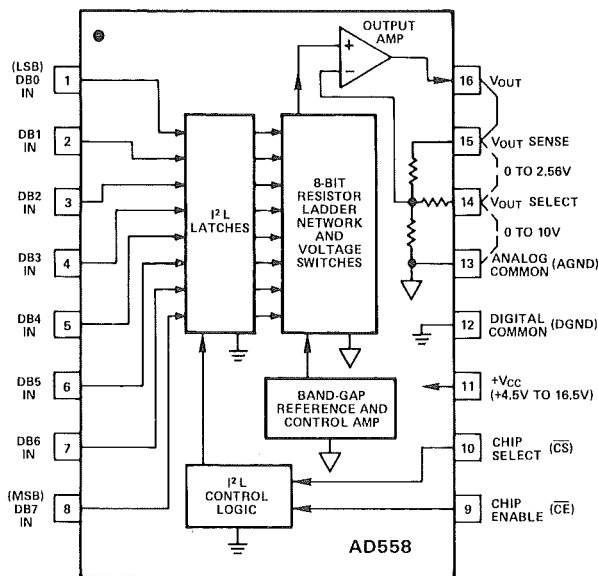


Figure 8.10. Block diagram of complete 8-bit bus-compatible d/a converter.

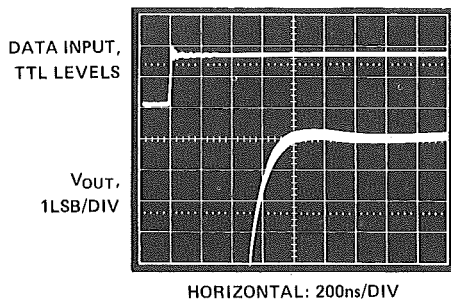


Figure 8.11. Detail of settling characteristic of 8-bit DAC for full-scale step, 2.56-V output range.

### *Keys to the Complete 8-Bit DAC*

The block diagram (Figure 8.10) shows the elements of the AD558, which was—and remains—a triumph of circuit design, processing, and trimming technology, much of it patented.

First, its design is fully integrated, rather than a collection of stock circuits. This results in a small chip (hence better yield and lower cost), low dissipation (hence better performance over temperature, and a wider range of applications), and a compact pinout (only 16 pins, hence improved reliability and a smaller footprint).

Second, the use of Bipolar/ $I^2L$ , bandgap-reference, and thin-film-on-silicon technologies provide these important benefits:  $I^2L$  (integrated injection logic) permits efficient use of a single chip for digital and high-performance analog circuitry; bandgap reference provides tracking reference voltage with low



tempcos, excellent long-term stability, and low- $V_{CC}$  operation; and thin-film-on-silicon permits stable, linear, trimmable resistors to be fabricated for high-accuracy conversion.

Finally, the device is automatically laser-trimmed at the wafer stage. This technology results in converters that are fully calibrated—ending rejections in expensive packages and requiring no user trims, even when bought as chips for use in hybrid circuits—and monotonic over the entire operating temperature range.

### *Easy to Interface*

The low-current logic inputs, set for TTL threshold voltage, can be operated by TTL or low-voltage CMOS over the entire operating  $V_{CC}$  range. The 100- $\mu$ A maximum current minimizes bus loading.

The input latches simplify interfacing to 8- and 16-bit data buses. The latches are controlled by  $\overline{CS}$  (Chip Select) and  $\overline{CE}$  (Chip Enable) inputs (as mentioned earlier), internally *nor*'d so that the latches transmit input data to the DAC section only when  $\overline{CS}$  and  $\overline{CE}$  are both at logic zero. When either of the control inputs goes to logic 1, the input data is latched into the registers and held until both are again returned to zero. If the application does not involve control of inputs from a common data bus, both control inputs can be tied to 0 for transparency.

The AD558 acts like a “write only” location in memory. It can double up with a ROM slot, with no interaction; or, if doubled up with read-write memory, the memory will retain the word written into the DAC and can read it back without disturbing the DAC. Typical connections to a  $\mu$ P are shown in Figure 8.12.

## 8.3 CMOS DACS

As mentioned, CMOS technology has emerged as a superior process for producing low-power logic functions. In addition, CMOS transmission gates can be used as switches for the analog signals in DACs and ADCs.

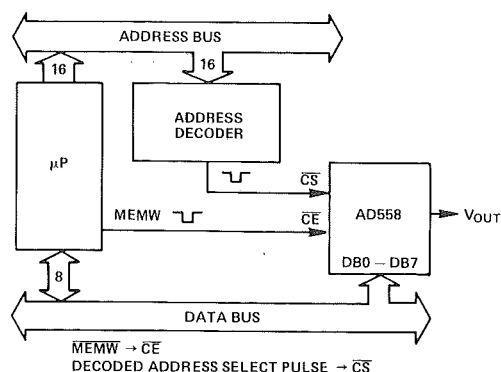


Figure 8.12. Typical microprocessor interface to 8-bit DAC.

The AD7520 10-bit multiplying DAC, introduced in 1974, was the first commercially produced CMOS DAC. It was the progenitor of an entire family of devices, from 8 to 16 bits in resolution, and including both D/A and A/D converters. The original design has since been revised to take advantage of smaller-geometry devices, and the AD7520 itself has been superseded by the AD7533.

### 8.3.1 CMOS D/A CONVERSION

Early commercially available monolithic d/a converters were principally processed by conventional bipolar linear processing techniques. Before 1974, when the AD7520 was introduced, 10-bit conversion had been difficult to obtain with good yields (and low cost) because of the finite  $\beta$  of switching devices, the  $V_{BE}$ -matching requirement, the matching and tracking requirements on the diffused-resistance ladders, and the tracking limitations caused by the thermal gradients produced by high internal power dissipation.

All of these problems were solved or avoided with CMOS devices. They have nearly-infinite current gain, eliminating  $\beta$  problems. There is no equivalent in CMOS circuitry to a bipolar transistor's  $V_{BE}$  drop; instead, a CMOS switch in the *on* condition is almost purely resistive, with the resistance value controllable by device geometry. The temperature-tracking problems of diffused resistors were solved easily: they weren't used.

The R-2R ladder is composed of 2-k $\Omega$ /square silicon-chromium resistors (a 10-k $\Omega$  resistor has a very manageable length/width of 5:1), deposited on the CMOS die. While the absolute temperature coefficient of these resistors is 150 ppm/ $^{\circ}$ C, their tracking with temperature is better than 1 ppm/ $^{\circ}$ C. The feedback resistor for the output amplifier is also provided on the chip to ensure that the DAC's gain-temperature coefficient is better than 10 ppm/ $^{\circ}$ C—by sidestepping the absolute temperature coefficient of the network.

Finally, the low on-chip dissipation of only 20 mW (including the dissipation of the ladder network), in conjunction with the excellent tracking capabilities of the thin-film resistors, minimizes linearity-drift problems caused by internally generated thermal gradients. Low dissipation also helps to minimize the power and cooling requirements for circuitry that the AD7520/AD7533 is used in.

Figure 8.13 shows a functional diagram of the d/a converter, which employs an inverted R-2R ladder. Binary-weighted currents flow continuously in the shunt arms of the network; with 10V applied at the reference input, 0.5 mA flows in the first, 0.25 mA in the second, 0.125 mA in the third, and so on. The  $I_{OUT1}$  and  $I_{OUT2}$  output buses are maintained at ground potential, either by operational-amplifier feedback, or by a direct connection to common.

The switches steer the current to the appropriate output lines in response to the individually applied logic levels. For example, a “high” digital input to SW1 will cause the 0.5 mA of the most significant bit (MSB) to add to  $I_{OUT1}$ .

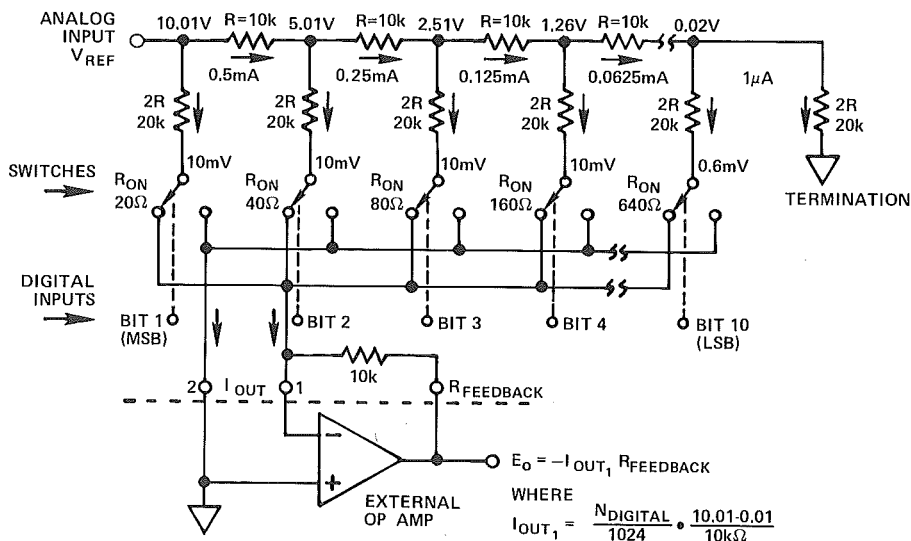


Figure 8.13. Functional diagram of CMOS d/a converter, with  $V_{REF} = 10.01$  V. Bits 5 through 9 of 10-bit device are omitted for clarity.

When the digital input is “low,” the current will flow through “ $I_{OUT2}$ .” If  $I_{OUT1}$  flows through the summing point of an operational amplifier and  $I_{OUT2}$  flows to ground, then “high” logic will cause the nominal output voltage of the op amp to be  $-(0.5 \text{ mA}) \times (10k\Omega) = -5\text{V}$ , for a positive reference voltage of 10V, while “low” logic will make the contribution of Bit 1 zero. With all bits *on* (i.e., “high”), the nominal output will be  $-9.99\text{V}$ . With all bits *off*, the output will be zero.

Linearity errors, and—more important—their variation with temperature, are affected by variations of resistance in both the resistors and the switches. As we have seen, the resistance-network tracking is excellent. However, it is natural to expect that the switches, while tracking one another, will not track the resistance network. With identical switches having realistic resistance values (say 100 ohms), one would expect that, as temperature changed, the variation of resistance in the series legs would transform the network into an  $R$ - $nR$  network, with  $n$  sufficiently different from 2 to destroy the binary character of the network and cause the converter to become non-monotonic.

The key to the linearity of the AD7520 is that the geometries of the switches are tapered so as to obtain *on* resistances that are related in binary fashion, for the first 6 bits. Thus, the nominal values of switch resistance range from 20 ohms for the first bit, 40 ohms for the second bit, through 640 ohms for the last 5 bits. The effect is, as can be seen in Figure 8.13, to provide equal voltages at the ends of the 6 most-significant arms of the ladder ( $0.5 \text{ mA} \times 20 \text{ ohms} = 0.25\text{mA} \times 40 \text{ ohms} = 10\text{mV}$ ). Since this drop is, in effect, in series with the reference, it causes an initial 0.1% scale-factor (“gain”) error, which

is well within the specifications but does not affect the linearity. Since the switches tend to track one another with temperature, linearity is essentially unaffected by temperature changes, and the gain drift is held to within the 10 ppm/°C specification.

Ten-bit linearity could, of course, have been obtained by scaling the *on* resistance of all the switches to a negligible value, say 10 ohms, but the switches would have required very large geometries, which would result in a 30 percent to 50 percent larger chip, at a substantial increase in cost.

Figure 8.14 illustrates one of the 10 current switches and its associated internal drive circuitry. The geometries of the input devices (1 and 2) are scaled to provide a switching threshold of 1.4V, which permits the digital inputs to be compatible with TTL and CMOS. The input stage drives two inverters (4 & 5, 6 & 7) which in turn drive the N-channel output switches.

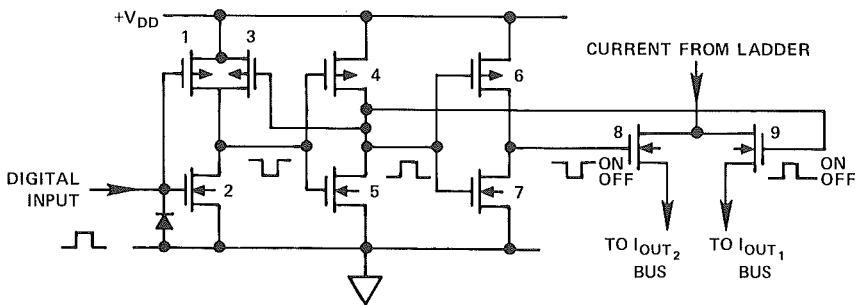


Figure 8.14. CMOS switch used in the AD7520 family. Digital input levels may be TTL or CMOS.

### 8.3.2 EQUIVALENT CIRCUIT

Figure 8.15 shows the equivalent circuit of the AD7533 at the two extremes of input, all inputs “high” (a), and all inputs “low” (b).  $V_{REF}$  (or  $I_{REF}$ , if a current reference is used) sees a nominal 10-k $\Omega$  resistance, regardless of the switch states. The current source,  $I_{REF}/1,024$ , represents a 1-LSB current loss through the 20-k $\Omega$  ladder-termination resistor, shown in Figure 8.13.  $R_{ON}$ , in this case, is the equivalent resistance of all ten switches connected to the  $I_{OUT1}$  bus (a) or the  $I_{OUT2}$  bus (b). Current-source  $I_{lkg}$  represents junction- and surface-leakage to the substrate. Capacitors  $C_{OUT1}$  and  $C_{OUT2}$  are the output capacitances-to-ground for the *on* and *off* switches.  $C_{SD}$  is the open-switch capacitance.

The 1,000:1 ratio between  $R_{ladder}$  and  $R_{ON}$  provides a number of benefits, all related to the small voltage drop across  $R_{ON}$ :

- $V_{REF}$  can assume values exceeding the absolute-maximum CMOS rating,  $V_{DD}$ . For example,  $V_{REF}$  could be as large as  $\pm 25V$ , even if the DAC's  $V_{DD}$  rating were only  $+17V$ .

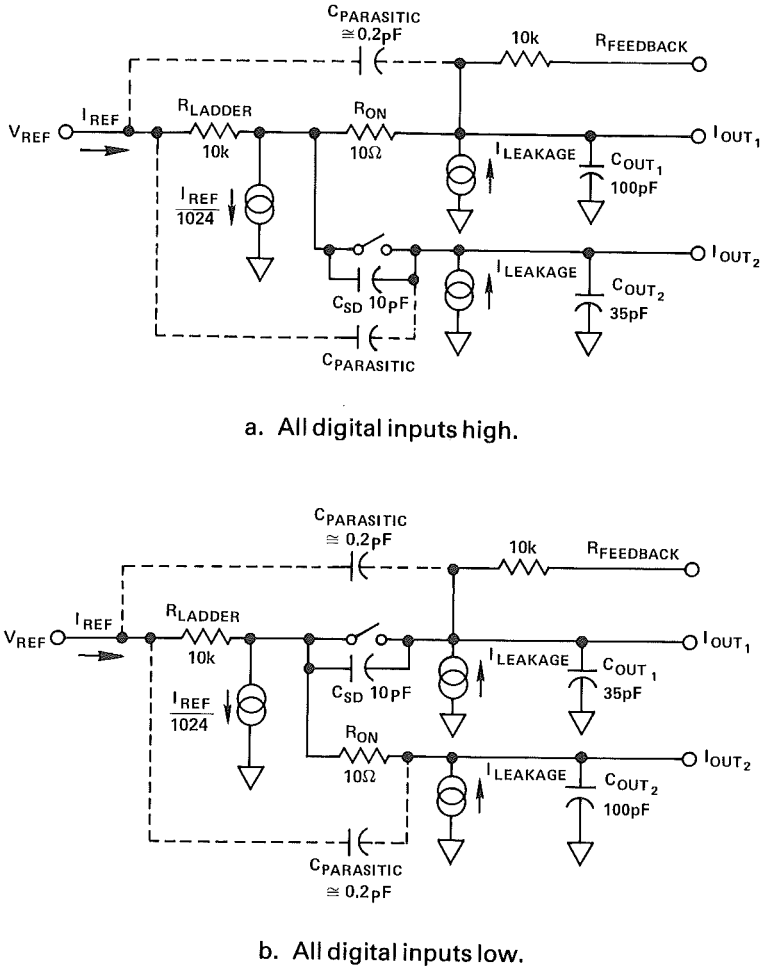


Figure 8.15. Equivalent circuits of 10-bit CMOS d/a converter.

- The nonlinearity temperature-coefficient depends primarily on how well the ladder resistances track. Since  $R_{ON}$  is only a small fraction of  $R_{ladder}$ , any  $R_{ON}$  tracking errors will be felt only as 2nd- and 3rd-order effects.
- The same argument holds true for power-supply variations. Any change of switch *on* resistance, as the power supply changes, will be swamped by the 1,000:1 attenuation factor. Power-supply rejection is better than 1/3 LSB per volt.
- If  $V_{REF}$  is a fast ac signal, the feedthrough coupling via  $C_{SD}$ , the open-switch capacitance, will be negligible, again because of the 1,000:1 voltage step-down. The parasitic capacitances from  $V_{REF}$  to  $I_{OUT1}$  and  $I_{OUT2}$  comprise the major source of ac feedthrough. Careful board layout by the user can result in less than  $\frac{1}{2}$  LSB of ac feedthrough at 100 kHz.

Since the *on* resistance depends only on value of  $V_{DD}$ , not the current through the switch, and the resistance network is unaffected by  $V_{REF}$ , the full-scale output current (all bits “high”) is nominally  $V_{REF}/10.01\text{ k}\Omega$ , less the “constant” current losses shown in Figure 8.15. This means that  $I_{OUT}$  is almost perfectly proportional to  $V_{REF}$  over the whole range from  $-10\text{V}$  to  $+10\text{V}$ . Equally important, the conversion linearity error (0.05%) is independent of the sign or magnitude of  $V_{REF}$ .

The extremely low analog-linearity error at constant digital input results in excellent fidelity to the input waveform, which suggests some interesting possibilities for the AD7520 family in the calibration and control of gain in signal generators, high-fidelity amplifiers, and response-testing systems.

The AD7520/7533 architecture is easily extended to 12-bit resolution by merely adding additional switch cells and resistors. However, in order to achieve consistent yields to 12-bit linearity, it is necessary to use error-correction techniques. The AD7541, the first CMOS DAC to offer 12-bit linearity and monotonicity, is schematically identical to the AD7520 and AD7533 with additional switches and resistors (Figure 8.16); but laser trimming at the wafer level adjusts the bit-weight ratios to the accuracy required for 12-bit performance.

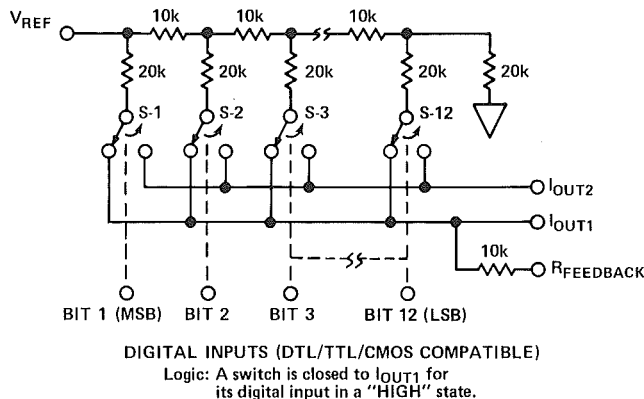


Figure 8.16. Functional block diagram of the AD7541 12-bit CMOS DAC.

### 8.3.3 DIGITAL BUFFERING

We have already pointed out that the great advantage of CMOS is the ability to embody complex logic functions without significantly increasing the chip's power dissipation. In a DAC, the most obvious logic function to add is the digital bus interface. As an example of what can be done, Figure 8.17 shows a family of bus-compatible 12-bit DACs based on the AD7541, each optimized for a particular bus architecture. The members of the family are:

DEVICE	INPUT WORD WIDTH	BUFFERING
	No. of Bytes $\times$ Byte Width	
AD7543	12 $\times$ 1 bit (bit-serial)	Double
AD7542	3 $\times$ 4 bits (nybble-serial)	Double
AD7548	1 $\times$ 4 bits and 1 $\times$ 8 bits (byte-serial)	Double
AD7545	1 $\times$ 12 bits (parallel)	Single
AD7549	Dual 3 $\times$ 4 bits (nybble-serial)	Double (dual DAC)

The AD7542 and 7543 are useful in applications where it is desirable to isolate the DAC from the rest of the system. With fewer input lines, the expense of wiring and optical isolators can be held to a minimum. Since these devices are housed in small 16-pin single-width DIPs, they require little board space, socket requirements are simplified, and system reliability is improved.

The AD7545 is designed to be used with 12-bit and wider buses. It accepts the 12-bit input word and applies it to the DAC inputs directly. In these applications, it is not necessary to use double-buffering on the chip.

The AD7548 is intended for use in systems where the data bus is 8 bits wide. The data can be presented to the DAC in either a right- or left-justified format in two bytes. This device, like the AD7542 and AD7543, uses double buffering to prevent the generation of spurious analog outputs from intermediate digital data.

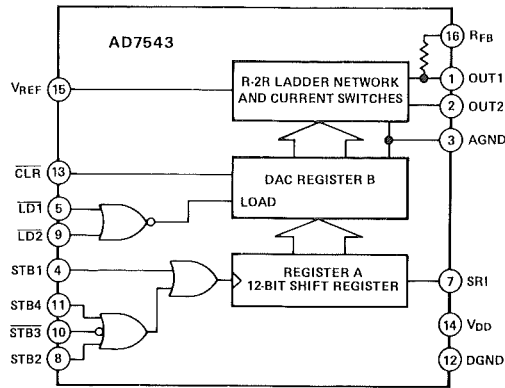
A dual DAC, the AD7549, in which two DACs share the same bus, uses the same 4-4-4 loading format as the AD7542, to allow the device to be packaged in a 20-pin (0.3") DIP.

#### 8.3.4 ANALOG CONSIDERATIONS

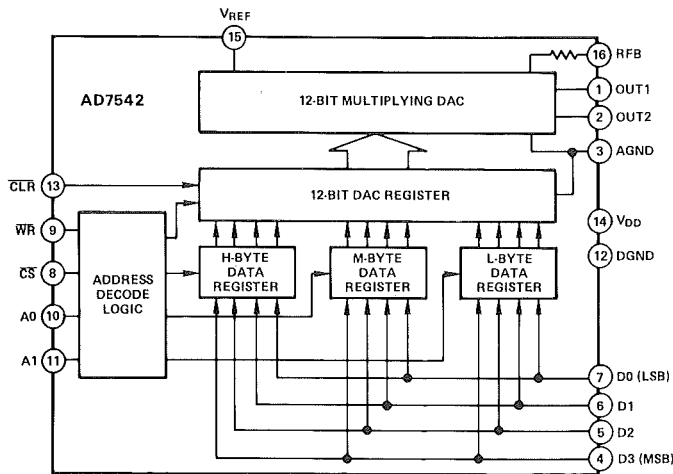
The *analog* connections for any of the CMOS DACs discussed above are essentially the same. The output terminals are designed to be operated into ground potential (or the virtual-ground terminal of an output op amp). The current from each bit that is turned on is directed to the  $I_{OUT}$  terminal, which is connected to the inverting input of an op amp. The output current flows through the on-chip feedback resistor (which matches and tracks the ladder resistors) to provide a voltage output at the output terminal of the amplifier.

It is important to note that the output amplifier must have low offset voltage in order to preserve the linearity of the converter's transfer function. This is a rare example of two parameters which are usually independent actually interacting. Figure 8.18 illustrates the nature of the problem.

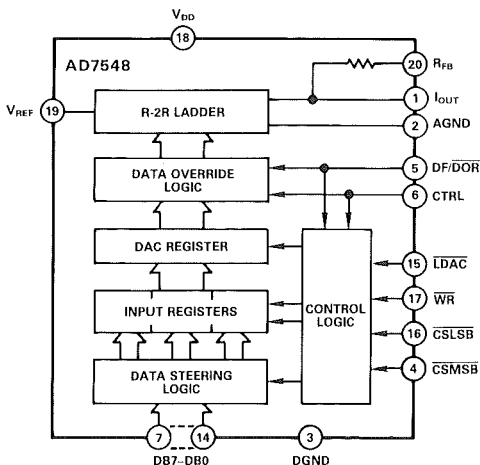
Inverted-ladder CMOS DACs—with characteristic ladder resistance,  $R$ —exhibit a code-dependent output resistance between ground and the amplifier summing point, varying from  $R$  to  $3R$  (and actually to infinity in the trivial case of all bits turned off). This output resistance variation is not linear with



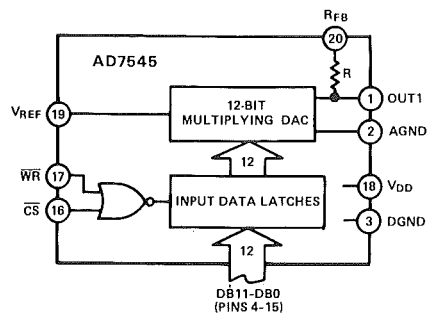
a. Serial-loaded, double-buffered DAC.



b. DAC with three 4-bit nibbles for 4-, 8-, or 16-bit buses.



c. DAC with 2-byte loading, either left- (8,4) or right- (4,8) justified, for 8-bit buses.



d. DAC with single-byte 12-bit parallel loading for 16-bit buses.

Figure 8.17. Architectures of bus-compatible 12-bit CMOS multiplying DACs.



code, since a single-bit code—other than the MSB—approaches  $3R$  output resistance, while codes with many bits turned on yield an output resistance which approaches  $R$ .

Since the amplifier is operating with a variable source resistance and a fixed feedback resistance (equal to  $R$ ), the “noise gain,” applied by the op amp to its own offset voltage, varies from  $4/3$  to  $2$ . Since the worst-case gain changes occur at the same codes as the worst-case differential linearity, it is important to keep the error term ( $2/3 V_{OS}$ ) much less than one LSB. Therefore, amplifiers with sub-millivolt offsets are required for 12-bit linearity.

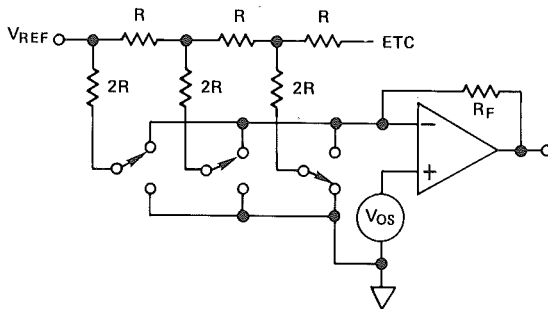
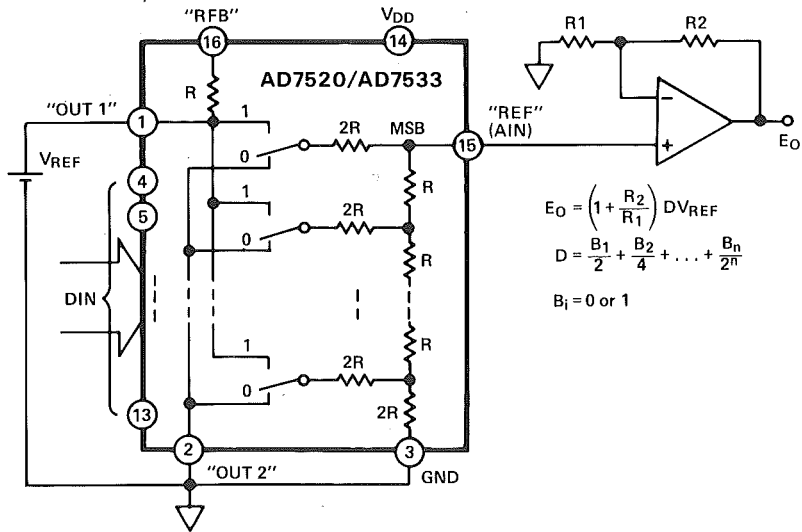


Figure 8.18. Modulation of op-amp circuit noise gain by CMOS DAC switches. In the case of  $V_{OS}$ , this can cause a code-dependent nonlinearity unless  $V_{OS}$  is negligible.

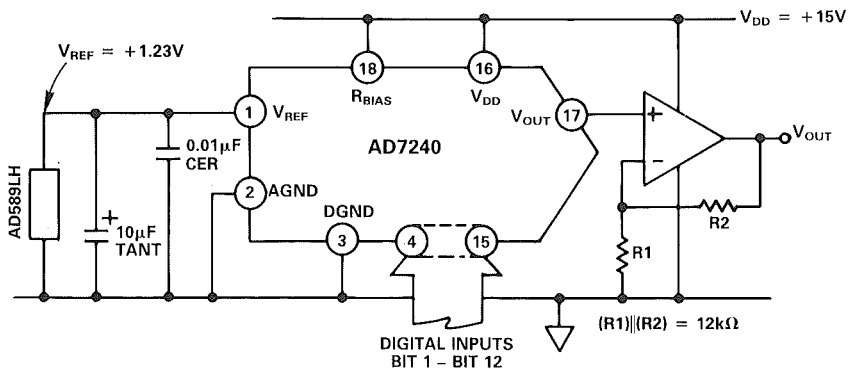
It is possible in some applications to circumvent the need for high-quality amplifiers by operating the DAC in a voltage-switching mode, rather than the current-switching mode (Figures 7.17 and 7.18). The AD7240 is designed to be used—and is specified for performance—in the voltage-switched mode (Figure 8.19).

In this mode, the terminal usually designated  $I_{OUT}$  becomes the reference input. The terminal usually designated REF IN becomes the voltage-output. This configuration removes the requirement for a low-offset output amplifier, since the DAC impedance seen by the amplifier input is constant (and equal to  $R$ ). In applications where the load resistance driven by the DAC is high relative to  $R$ , no buffering is needed. However, if lower impedance loads must be driven, an amplifier configured as a voltage follower can be used. The voltage source connected to the reference input should have low dynamic impedance, since it must drive a switched load.

This mode of operation offers another benefit. It is possible to operate a CMOS DAC in the voltage-switching mode on a single power supply. However, the reference voltage range is small compared to that of current-switching DACs. The AD7240, for example, is rated for 12-bit linearity for a reference voltage of 1.2 Volts.



a. General principle.



b. Application of the AD7240 voltage-switched DAC.

Figure 8.19. Using a CMOS DAC in the voltage-switched mode.

Higher reference voltages will cause degraded linearity due to the reduced drive available for the CMOS switches. The DAC is trimmed with the assumption that the gate-to-source voltage is large. Since the gate is driven to the positive-supply level, and the source is tied to the reference input, it can be seen that an increased reference will cause problems. Furthermore, only a positive reference can be used in this mode. A negative reference will forward-bias a parasitic transistor in the DAC and could result in damage to the device. This is not usually a problem in systems which use only a single positive power supply.

The CMOS DACs discussed above all require *external* op amps in the current-switching mode, and also—if buffering is required—in the voltage-switching mode. As noted earlier, the chief disadvantage of using CMOS technology to manufacture converter circuits is that the analog components (amplifiers, references, etc.) have traditionally been of poor quality. CMOS references, for example, generally exhibit higher noise and drift than bipolar devices. Amplifiers made from CMOS have suffered from poorer noise, drift, and output drive capability than bipolar units (the exception is the CMOS chopper-stabilized type, which has very low offset drift—but it still has more noise and lower drive capability than a bipolar type).

In many CMOS processes, a parasitic NPN transistor is formed, and great effort is expended in order to minimize its effect on the circuit. However, in the Analog Devices LC<sup>2</sup>MOS (linear-compatible CMOS) process—specifically developed to permit both high-speed digital logic and precision analog circuits to be integrated on the same chip—the NPN transistor, used to great advantage, is the key to a DAC output amplifier with lower noise and higher drive capability than a pure CMOS device.

The single-supply 8-bit voltage-output DAC, shown in Figure 8.20, is an example of the performance achievable with the LC<sup>2</sup>MOS process. The AD7224 is a monolithic 8-bit CMOS microprocessor-compatible d/a converter in an 18-pin dual in-line package. Designed for a variable or fixed external reference, it is a complete voltage-output device, with double-buffered data inputs and an on-chip output amplifier. Because of its low total unadjusted error—less than 1 LSB over temperature (L, C, and U grade)—it requires no adjustments.

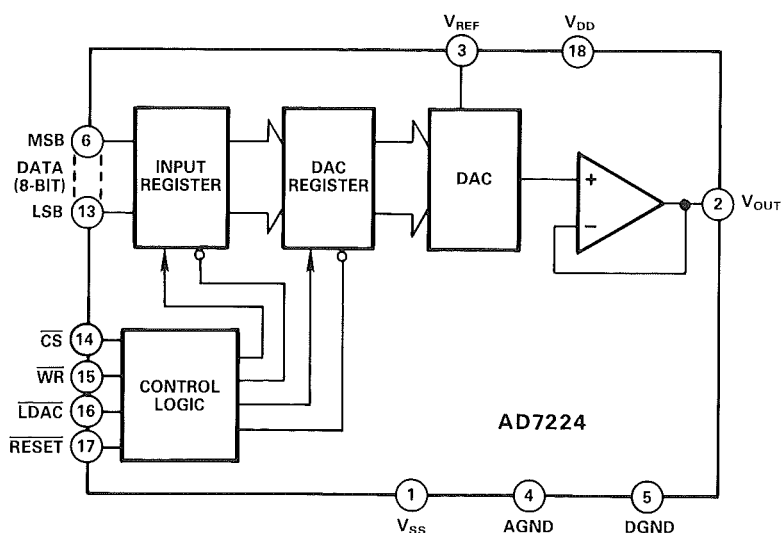


Figure 8.20. Functional block diagram of 8-bit, voltage-output CMOS DAC.

Its high-speed logic allows direct interfacing to most microprocessors. The double-buffered interface logic consists of an input register and a separately enabled DAC register. This arrangement allows the input register to be updated at the convenience of the microprocessor, while the DAC is updated whenever necessary. As a result, a number of DACs can be primed separately by the microprocessor, without changing their existing output levels, then enabled to deliver their new outputs simultaneously, or in a required sequence, a useful feature in (for example) test equipment.

A low-dissipation device (typically 35 mW with a single supply), it will operate with either a single positive supply and a +10-volt reference, or dual supplies and a +2-volt to +12.5-volt reference. The output amplifier can develop 10 volts across a load of 2 kilohms. The device is available in six grades, three temperature ranges, and 3 packages (including plastic).

### 8.3.5 MULTIPLE CONVERTERS

As low-cost converters have become increasingly more available, their use has grown and they have made many new applications possible. Often, it is cost-effective to add a converter in order to make an additional system feature available. On the other hand, it is desirable to reduce the physical size of systems as much as possible. New IC packaging technologies are evolving, but they are being primarily applied to digital circuits. Most linear and converter circuits have performance that is more sensitive to packaging, and they have remained in classical IC packages. Thus, the system designer is faced with the problem of adding increasing numbers of converters in relatively large packages.

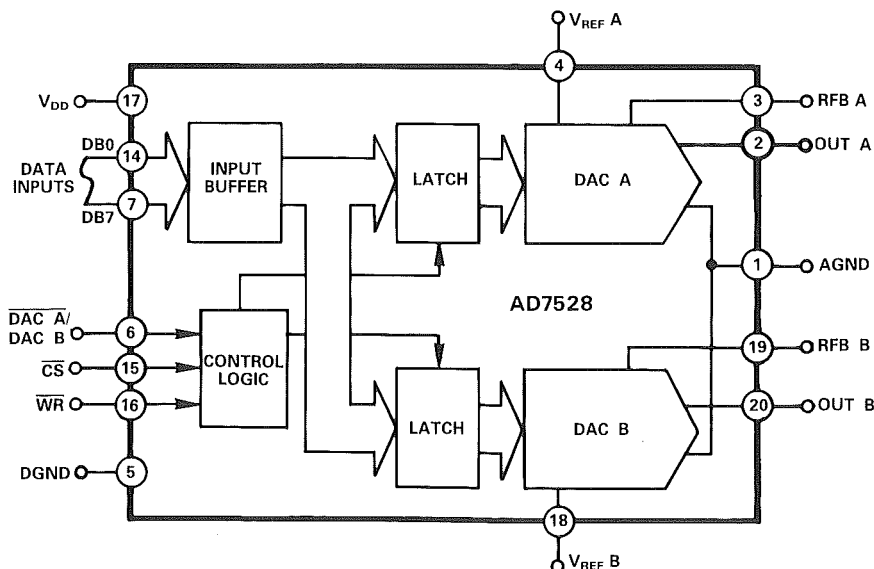


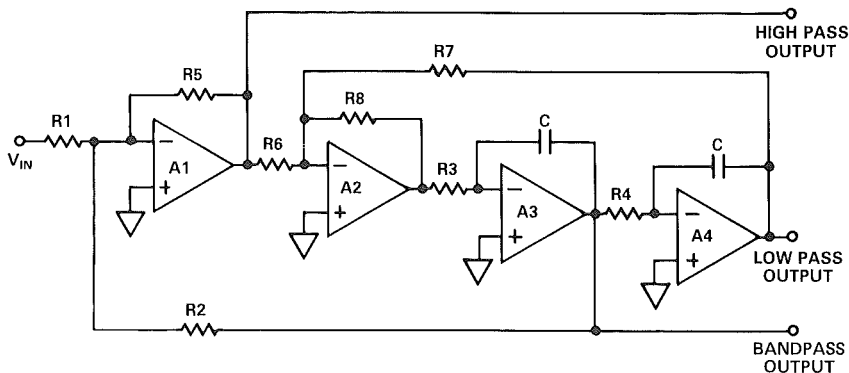
Figure 8.21. Functional block diagram of dual 8-bit monolithic DAC.

In the interest of improving circuit density in systems using many DACs, several multiple-DAC products have evolved. The task of packaging multiple devices on a monolithic chip or hybrid substrate has been made easier by the number of shared elements, from power supply to data and control buses. These have made it unnecessary to substantially increase the pin count of the chip or package each time a device is added.

The earliest, designated the AD7528 (Figure 8.21), is a dual 8-bit current-output device housed in a 20-pin single-width dual in-line package (DIP). The ladder resistances of the two DACs are tightly matched in this device, a useful feature in many applications. For example, it is possible to use the AD7528 in a digitally tuned state-variable filter.

### Filter Application

The state-variable filter (or universal filter, as it is often called) is a convenient second-order filter block. It provides simultaneous low-pass, high-pass and bandpass outputs. All filter parameters can be readily adjusted. Figure 8.22 shows a typical filter circuit with expressions for center frequency,  $Q$ , and gain for the bandpass output.



#### BANDPASS TRANSFER FUNCTION

$$\frac{V_{OUT}}{V_{IN}}(f) = \frac{A_0}{1 + jQ \left[ \frac{f}{f_0} - \frac{f_0}{f} \right]}$$

Where  $f$  = input frequency of  $V_{IN}$

$A_0$  = gain at  $f = f_0$

$Q$  = circuit  $Q$  factor, i.e.,  $\frac{f_0}{3\text{dB Bandwidth}}$

$f_0$  = resonant frequency.

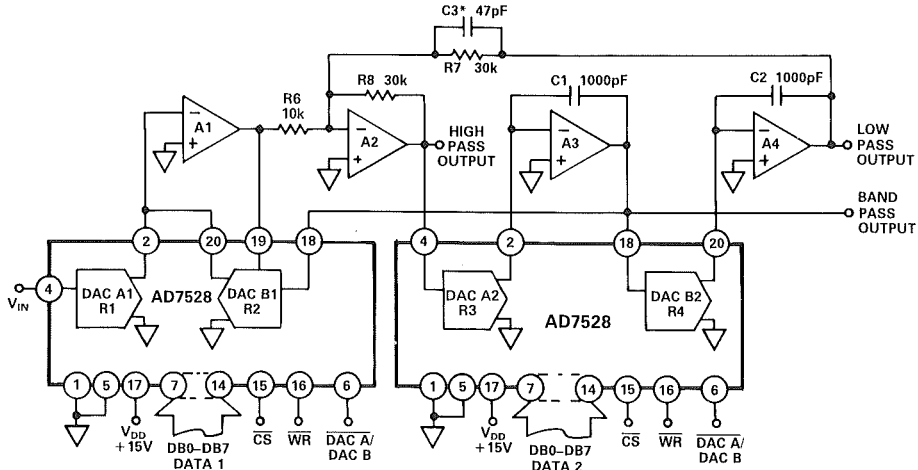
$$f_0 = \frac{1}{2\pi R_3 C} \cdot \sqrt{\frac{R_8}{R_7}} \quad (R_3 = R_4)$$

$$Q = \frac{R_6}{R_8} \cdot \frac{R_2}{R_5} \cdot \sqrt{\frac{R_8}{R_7}}$$

$$A_0 = -\frac{R_2}{R_1}$$

Figure 8.22. State-variable filter.

**DACs As Parameter-Control Elements.** If R1, R2 and R3, R4 are functionally replaced with matched DAC pairs the filter parameters can be made programmable, as shown in Figure 8.23. DACs A1 and B1 control filter gain and Q, while DACs A2 and B2 control center frequency ( $f_o$ ).



**NOTES:**

\*C3 IS A COMPENSATION CAPACITOR TO ELIMINATE Q AND GAIN VARIATIONS CAUSED BY AMPLIFIER GAIN BANDWIDTH LIMITATIONS

\*\*R5 IS REPLACED BY DAC B1 INTERNAL RFB  $\approx 11k\Omega$ , OP-AMPS ARE 2  $\times$  AD644. FOR COMPONENT VALUES SHOWN PROGRAMMABLE RANGE IS  $Q = 0.3$  TO 4.5,  $f_o = 0$  TO 15kHz.

**CIRCUIT EQUATIONS:**

$$C_1 = C_2, R_3 = R_4, R_7 = R_8$$

$$f_o = \frac{1}{2\pi R_3 C_1}$$

$$Q = \frac{R_6}{R_8} \cdot \frac{R_2}{R_5} **$$

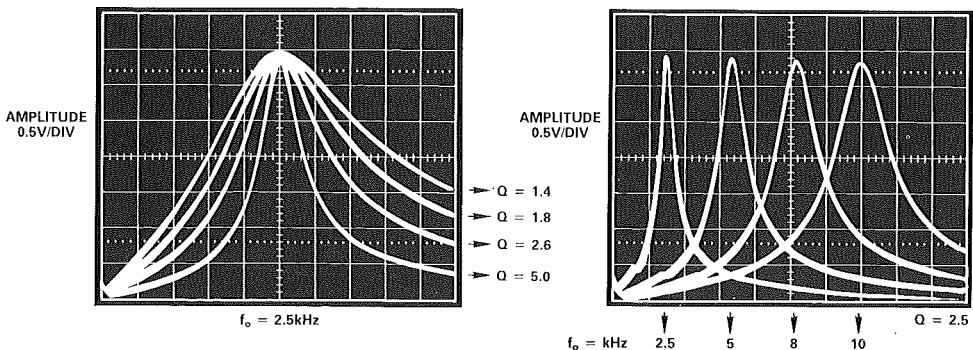
$$A_O = -\frac{R_2}{R_1} \text{ For Bandpass Output}$$

DAC EQUIVALENT RESISTANCE EQUALS

$$\frac{256 \times (\text{DAC LADDER RESISTANCE})}{\text{DAC DIGITAL CODE (DECIMAL)}}$$

Figure 8.23. Digitally controlled state-variable filter.

For the component values shown, the programmable range of Q is from 0.3 to 4.5 and is independent of  $f_o$  (Figure 8.24a). Center frequency ( $f_o$ ) is programmable from 0 to 15 kHz (Figure 8.24b) and is independent of Q.

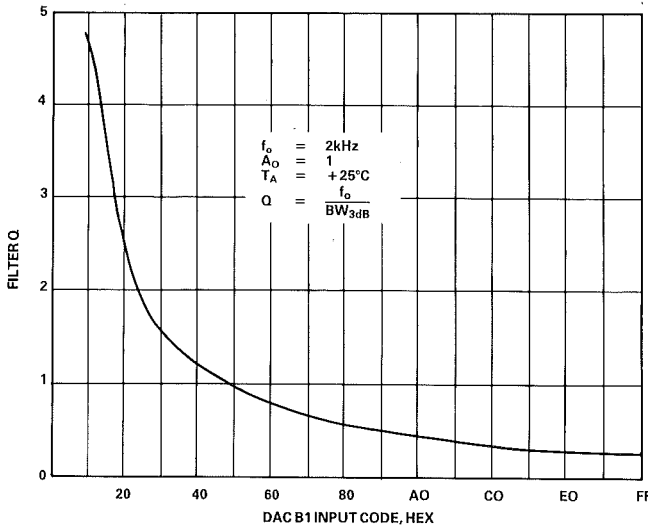
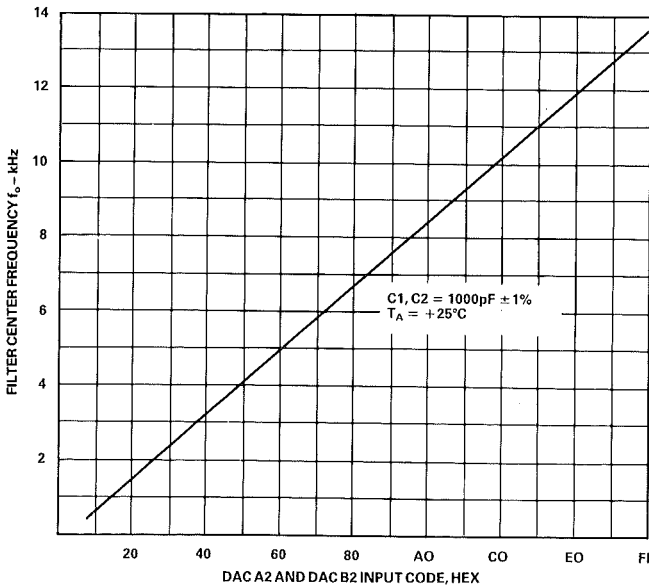


a. As a function of Q setting.

b. As a function of  $f_o$  setting.

Figure 8.24. Filter amplitude vs. frequency.

**Programming the Parameters.** Since maximum digital gain setting corresponds to minimum resistance, the input codes will be inverse with resistance value for a given parametric effect. The graph in Figure 8.25a shows how the circuit  $Q$  varies with DAC B1's input code (proportional to  $R_2$ , inverse with DAC B1 gain); and Figure 8.25b shows how the center frequency varies with DAC 2 (A and B) code for the component values given in Figure 8.23 (inverse with  $\sqrt{(R_3 \times R_4)}$ , direct with  $\sqrt{(A_2 \times B_2)}$  gains).

a.  $Q$  vs. code.b.  $f_o$  vs. code.Figure 8.25. Filter  $Q$  and  $f_o$  as a function of parameter values, expressed in hex code.

Gain variation alone, without affecting other parameters, is accomplished by changing DAC A1's input code. Unity gain occurs when the data in DAC A1 and DAC B1 latches is identical. Since the device's logic inputs are TTL or CMOS compatible, the DACs are readily interfaced to most microprocessors, thus providing an ideal microprocessor-control interface.

### Quad Voltage-Output DAC

In applications where the DAC is being used strictly as a digitally controlled voltage source, rather than as a digitally programmable resistor replacement, a dedicated voltage-output unit is generally preferred. As an example of a multiple voltage-output 8-bit DAC, Figure 8.26 shows the architecture of the AD7226 quad 8-bit DAC, housed in a 20-pin single-width DIP.

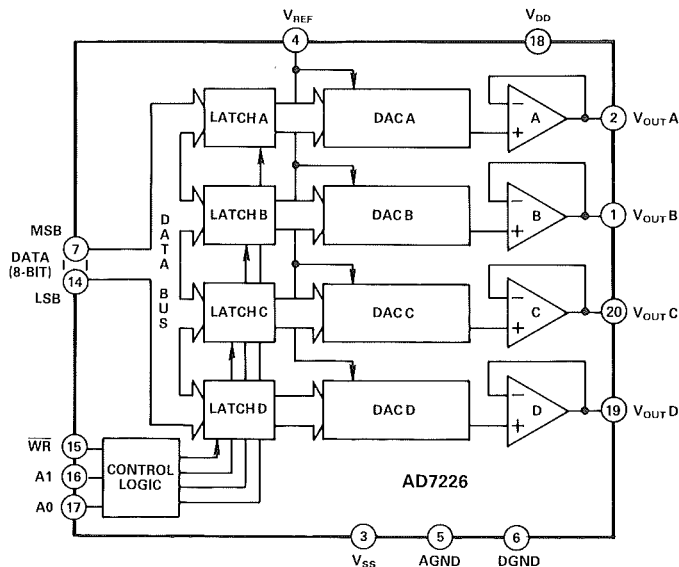


Figure 8.26. Functional block diagram of quad 8-bit CMOS DAC.

The four sets of latches are loaded via a common 8-bit data bus, under the control of two address bits (A0, A1) and an active-low WRITE pin (WR). All logic inputs are level-triggered and compatible with both TTL and CMOS (5-volt). Because its logic-interface circuitry operates at high speed, the AD7226 is compatible with most 8-bit microprocessors; typically, all four channels can be updated at 2 MHz, and a single channel can be updated at 8 MHz.

Each converter consists of an 8-bit R-2R ladder and its associated switches, connected for operation in the voltage mode (Figure 8.27). The output of each DAC is buffered by a short-circuit-protected on-chip CMOS follower amplifier, capable of driving up to 5 mA of output current. Because the device operates in the voltage mode, with non-inverting buffers, a single supply ( $V_{DD}$ ) from +11.4 V to +16.5 V may be used for unipolar output. The table shows the reference and output ranges for linear operation at each nominal supply-





Segmentation (see Figure 7.15) can be used in either the voltage or current mode. Its use in improving DAC resolution is somewhat easier to visualize when considered in the voltage mode.

In Figure 8.28, the 4 most significant bits of the input word are decoded to select one of 16 segments of the reference voltage,  $V_{REFH} - V_{REFL}$ , defined by a pair of adjacent taps on a string of 16 resistors. To  $V_{REFL}$  must now be added the fraction of the segment determined by the 12 lower bits. The chosen segment is buffered and applied to a second voltage division—this time by a 12-bit R-2R-type DAC, operated in the voltage mode; the position within the segment is selected by the lower 12 bits of the input digital word. The fraction of the segment thus chosen, added to  $V_{REFL}$ , gives the total output.

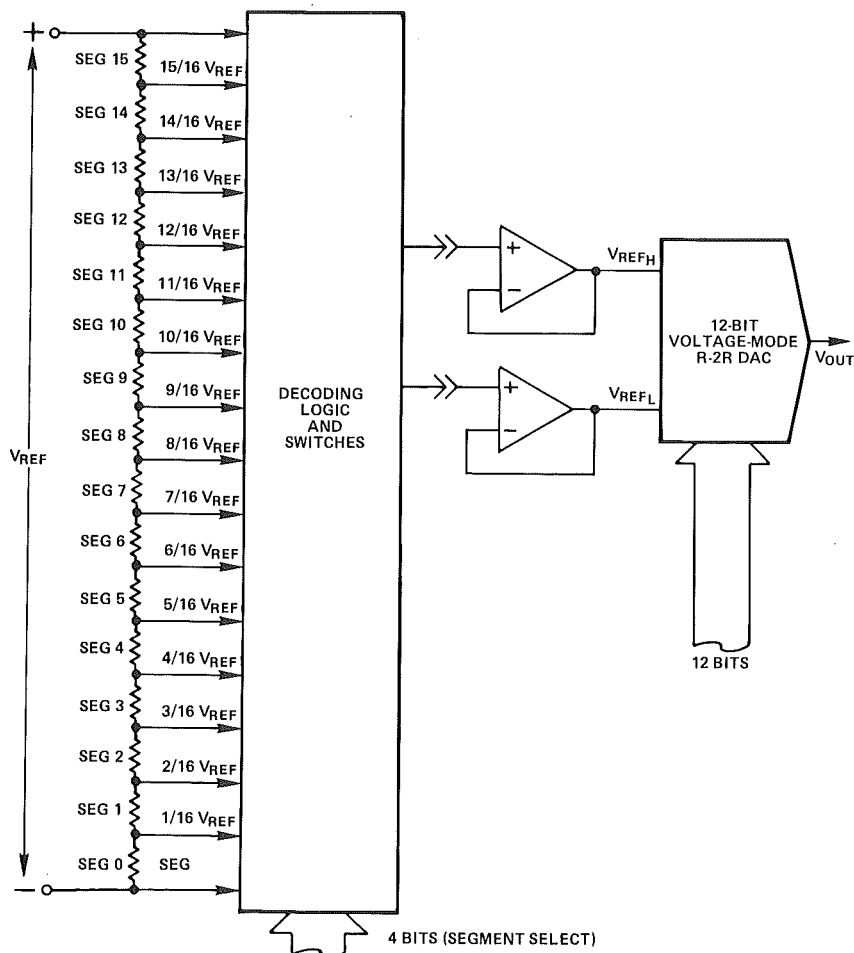


Figure 8.28. 16-bit segmented DAC architecture.

This voltage-segmentation technique was first used in the AD7546, a 16-bit monolithic voltage-output DAC with broadside input data latches for interfacing to 16-bit microprocessors (Figure 8.29). It employs a 12-bit R-2R DAC, operated in the voltage switching mode and supplied with a reference

voltage from a 4-bit segment DAC under the control of the four most-significant bits. A monolithic CMOS device, the AD7546 offers outstanding differential-nonlinearity specifications, headed by  $\pm 0.0015\%$  (16-bit monotonicity) for premium grades. An on-chip analog switch, synchronized with the latch loading signal, is provided for use with track/hold circuits for deglitching.

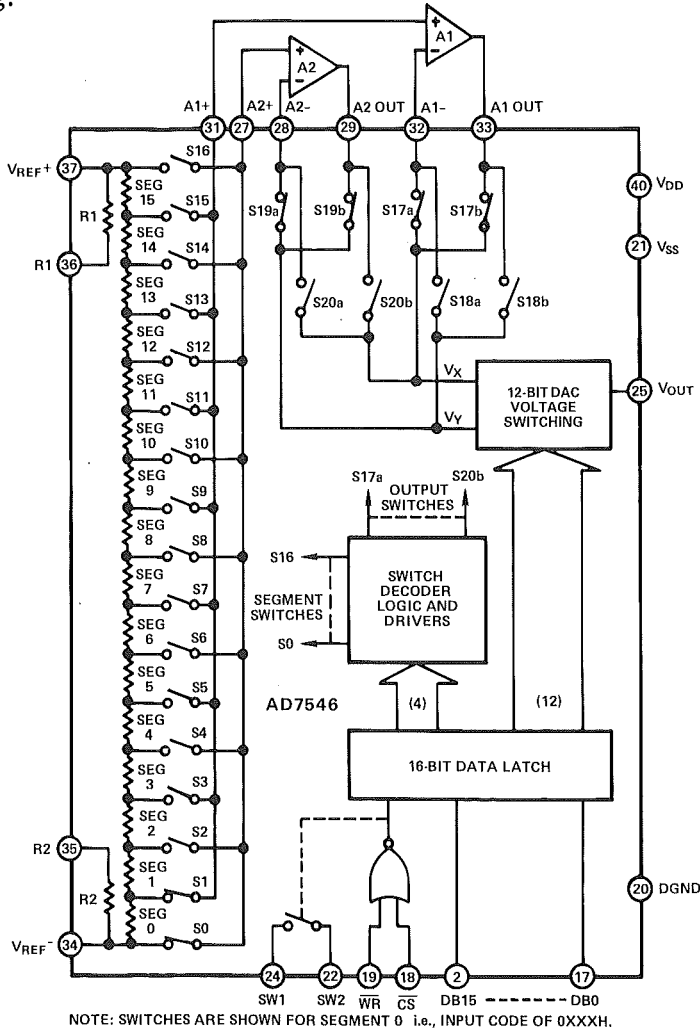


Figure 8.29. Functional block diagram of 16-bit segmented DAC.

The top four bits are decoded to select, via the segment switches, one of the 16 voltage segments available along the resistor chain. This voltage segment,  $(V_{REF+} - V_{REF-})/16$ , is buffered by external follower amplifiers and used as a voltage reference for a 12-bit R-2R-type d/a converter operating in the voltage switching mode. When the segment voltage is applied to  $V_X$  and  $V_Y$ , the output of the d/a converter may be expressed as follows:

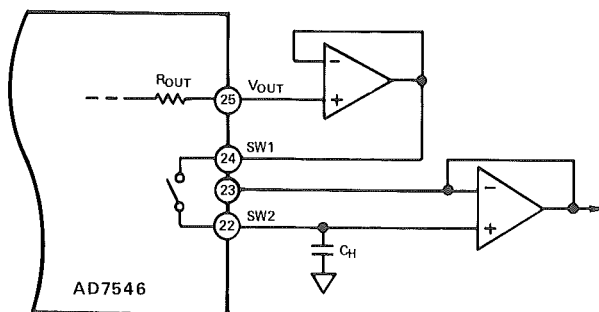
$$V_{OUT} = V_Y + D(V_X - V_Y) \quad (8.1)$$

where  $D$  is the fractional analog value of the lower 12-bit digital code,  $V_X$  is the upper segment voltage and  $V_Y$  is the lower segment voltage. The 12-bit d/a converter's reference inputs,  $V_X$  and  $V_Y$ , are connected to the two buffered resistor-chain nodes, which define the segment of interest; the 12-bit DAC interpolates between the voltages at these two points.

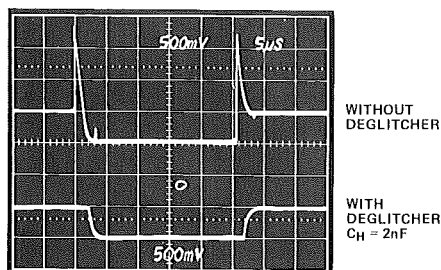
In this way, the 65,536 output levels available from the 16-bit DAC are divided into 16 groups of 4,096 steps each. Since the largest output value from the 12-bit DAC doesn't exceed the minimum value of the next segment, the 16-bit DAC has to be monotonic—if the 12-bit DAC is itself monotonic. Thus, the monotonicity of the 16-bit DAC is limited by that of the resistance-ladder 12-bit converter; while these devices are reliably manufacturable with good yields, ladder-type converters for higher resolutions, approaching 16 bits are not yet fully feasible—hence the use of two-stage conversions.

The AD7546 has a 16-bit-wide internal latch to facilitate microprocessor interface. Signals  $\overline{CS}$  and  $\overline{WR}$  have the same interpretation (*chip select* and *write*) as in normal microprocessor systems. When both  $\overline{CS}$  and  $\overline{WR}$  are low the input latches are transparent, and the DAC output voltage follows the input data. With  $\overline{CS}$  low, the input data is latched on the rising edge of  $\overline{WR}$ .

Also included on the chip is an SPST switch intended for use in a track-and-hold circuit to remove glitches from the DAC output and simplify low-pass filtering of the reconstructed output voltage. The switch is synchronized with the latch loading signals; it is open when both  $\overline{CS}$  and  $\overline{WR}$  inputs are low. The



TRACK/HOLD CIRCUIT



TYPICAL OUTPUT WAVEFORMS USING THE TRACK/HOLD CIRCUIT

Figure 8.30. Deglitching a 16-bit DAC.

internal logic of the AD7546 ensures that the switch opens before data to the latches can change.

To function as a track-hold, the switch is connected in series with the DAC output, as shown in the Figure 8.30, with pin 24 as the input and pin 22 as the output. Pin 23 is a pin with no internal connections; its purpose is to serve as a guard. It should be connected to the output to minimize any feedthrough resulting from stray capacitances at the two switch terminals. When the switch is open, the Hold capacitor stores the previous output voltage of the DAC. The  $\overline{WR}$  pulse should be of sufficient duration to allow the DAC to settle to its new analog output and for all glitches to have settled out. Driving the  $\overline{WR}$  input from a one-shot will ensure sufficient settling time.

It is interesting to note that the external amplifiers used with the AD7546 need not be particularly accurate to preserve monotonicity. Switches S17-20 are used to insure that the same amplifier that buffers the top of one segment is also used to buffer the bottom of the next segment. Thus, the transfer function of the DAC remains monotonic, even if the amplifiers have large offsets. However, integral linearity will be degraded by large amplifier offsets, since—depending on which segment is selected—the size of each segment will be equal to the nominal segment size, plus or minus the difference of the op-amp offsets.

In the AD7546, the amplifiers are left as external components to be added by the user, since amplifiers with sufficiently low noise for 16-bit applications, not possible with the CMOS process technology of the early 1980s, could not be integrated on the same chip as the rest of the DAC circuit.

## 8.4 BiMOS DAC TECHNOLOGY

In addition to the use of standard bipolar and CMOS technologies in the manufacture of IC data converters, the new combinational technologies, BiMOS II and  $LC^2MOS$ , have been chosen to implement some of the new high-resolution converters at Analog Devices. The table outlines the relative strengths and weaknesses of the various technologies.

While development is under way on many general-purpose converters using  $LC^2MOS$  or BiMOS II, at this writing, existing designs are still implemented in bipolar and CMOS. Bipolar seems to be more capable of high accuracy and long-term stability, but CMOS is more versatile, in that it can operate more easily in a 4-quadrant multiplying mode. Bipolar devices are typically faster, but CMOS devices require much less power. The bipolar process has more versatile analog components available, for implementing reference circuits and amplifiers, but the CMOS process has high-quality digital components available for implementing on-chip logic, control, and storage functions.

The Analog Devices BiMOS process is an advanced, all-implanted, n-well process, which offers a combination of both high-speed-low-power CMOS

logic and high-speed-low-noise analog circuitry. It is ideally suited to the manufacture of monolithic data converters, since complex digital functions and high-precision linear circuitry can both be included on a single chip. The first product manufactured with this process was the AD569 16-bit DAC. Like the CMOS AD7546, it uses the segmented architecture to achieve 16-bit monotonicity, but with less-stringent matching requirements in the resistor network (Figure 8.31).

### COMPARISON OF IC DAC TECHNOLOGIES

	BIPOLAR	CMOS	BiMOS II	LC <sup>2</sup> MOS
Switches				
Speed	Excellent	Good	Good	Good
Stability	Excellent	Fair	Good	Good
Accuracy	Excellent	Good	Good	Good
Power	High	Very Low	Very Low	Very Low
Resistors				
Diffused Silicon	Fair	Fair	Fair	Fair
Deposited Thin Film	Excellent	Excellent	Excellent	Excellent
References	Excellent	Poor	Good	Fair
Multiplying Capabilities	Poor	Excellent	Excellent	Excellent
Amplifiers				
Speed	Excellent	Poor	Excellent	Good
Accuracy	Good	Poor	Excellent	Good
Logic				
Speed	Good	Good	Good	Good
Power	Poor	Excellent	Excellent	Excellent
Size	Fair	Good	Good	Good

The AD569 has two cascaded 8-bit resistor strings, each with 256 taps. The 8 most significant input bits select the segment of the first string, and the lower 8 bits select the tap within that segment by use of the second resistor string. Since it is only necessary that each string be monotonic to 8 bits, resistor matching requirements are easily achieved without trimming of any kind. Thus the AD569's transfer function is monotonic to 16 bits without trimming of any kind. Integral linearity error is held to less than 0.02%.

Gain and offset errors are minimized in the AD569 by use of separate force-sense connections between the reference and the first resistance divider. Without these Kelvin connections, errors would arise from the parasitic resistances encountered in circuit-board tracks, package pins, and internal bond wires. While these errors may seem small, it is important to remember that, at 16 bits, 1 LSB on a 10-volt span is a mere *153 microvolts*.

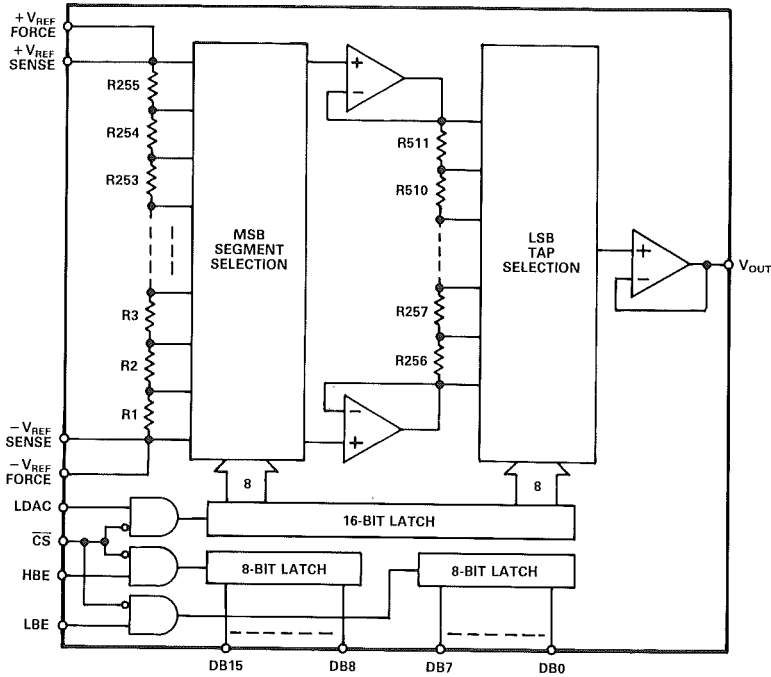


Figure 8.31. Double-buffered sixteen-bit monolithic d/a converter.

Unlike the AD7546, the AD569 includes high-precision buffer amplifiers on the same chip. These amplifiers reject common mode and achieve extremely high linearity in the follower mode by the use of a new circuit architecture which uses both bipolar and MOS transistors. Speed is not compromised in these amplifiers—output settling to 0.001% is typically 6 microseconds for a full-scale step. Furthermore, the AD569 can be used in a multiplying mode with reference signals of up to several hundred kilohertz.

The logic interface of the AD569 includes a set of double-buffered input registers. The control signals allow the first rank registers to be loaded from either an 8-bit or a 16-bit bus, followed by a transfer of the data from the first rank to the second.

The latches are controlled by four input signals: high-byte enable (HBE), low-byte enable (LBE), and load DAC (LDAC), all of which are internally gated with chip-select (CS). All control signals are compatible with all standard 5-volt logic families. The functioning of the control signals is shown here:

CS	LBE	HBE	LDAC	OPERATION
1	X	X	X	None—DAC Deselected
0	0	1	1	Load first-rank low-byte latch
0	1	0	1	Load first-rank high-byte latch
0	1	1	0	Load second-rank latch from first rank

The control signals can be tied together and more than one latch can be enabled at one time. For example, when loading directly from a 16-bit wide bus, HBE and LBE may be tied together and both latches enabled simultaneously.

## 8.5 HYBRID DACS

Digital-to-analog Converters have participated in a general progression from board (or module) form to hybrids, and then to monolithics. Hybrid and monolithic technologies share much in common—package size and manufacturing costs are similar and compare favorably with assembly of the DAC function in discrete form, as well as providing much higher reliability.

Hybrid construction allows several technologies to be combined in a single small package to provide a function which cannot be implemented in any existing monolithic technology. For this reason, it is unlikely that the advent of future IC technologies will bring about the demise of hybrids. Instead, hybrid suppliers will be able to combine these new technologies with other, older IC technologies in order to provide more-complex functions in a small physical area. Simply stated, the availability of more-advanced and more-powerful IC processes will make possible more-advanced and more-powerful hybrids.

For example, consider the evolution of the 12-bit DAC function. The first mass-produced modular 12-bit DACs consisted of a large number of discrete components to implement the various building blocks, such as switches, output and reference amplifiers, and resistance ladders. As monolithic technology progressed, operational amplifiers and arrays of matched switching transistors and level shifters became available in monolithic form. Thin-film resistor networks also became available. These were then used in modular converters to improve reliability and reduce manufacturing costs. Available in unpackaged chip form, these IC functional building blocks fostered economical manufacture of hybrid converters that were functionally as complete as the modules but with higher reliability and requiring much less physical space.

One of the most-popular 12-bit DACs is the DAC80, now available from several manufacturers in monolithic form (Figure 8.7). The original DAC80 was introduced in the mid-1970s as a hybrid device comprising 11 chips in a hybrid package. The 11 chips were: three 4-bit switch arrays, two operational amplifiers, two resistor networks, a Zener diode in chip form, two clamp diodes, and a chip capacitor. In 1978, when monolithic technology had progressed to the point where it was possible to combine the switch and resistor network functions on a single chip, a three-chip DAC80 was introduced. The three chips in this design included a reference chip, an output amplifier, and the switch/resistor/control-amplifier chip.

The newer design offered performance identical to that of the original DAC80, but with a tremendous improvement in reliability and at much lower cost.



Then, in 1983, the first single-chip DAC80 became available. It, of course, provided further cost reduction and reliability improvement, compared to the three- and eleven-chip hybrid versions. Finally, in 1984, this popular device was offered in a low-cost plastic DIP package. Thus, the DAC80 has evolved from a relatively high-cost hybrid to a high-volume commodity IC.

While this evolution is often used as an example to show the impending obsolescence of hybrid manufacturing, it is important to remember that the single-chip DAC80 can be used in chip form in hybrid designs. When combined with devices which are incompatible with the IC process used to produce the DAC chip (such as high-power drivers or MOS memory or logic functions), it is possible to produce more-complex functions in a package whose size is comparable to the monolithic, increasing the functional density available to the system designer.

A good example of the increase in functional density made possible by hybrid technology is found in the AD390 Quad DAC (Figure 8.32), which is based on the AD567 monolithic current-output DAC with its on-chip latches. The AD567 DAC chip requires only an op amp to convert the output current to a buffered output voltage. Normally, the AD567 is housed in a 28-pin DIP package. However, the AD390 contains *four of these DACs and their output amplifiers*, as well as an additional op amp to buffer the reference input, in a package which is the same size as a single AD567. Six address inputs allow any of the DAC registers (or any combination of registers) to be loaded from a 12-bit parallel bus.

The truth table indicates the functions available for various combinations of levels on the control bus.

CS1	CS2	CS3	CS4	A1	A0	Operation
1	1	1	1	X	X	No Operation
X	X	X	X	1	1	No Operation
0	1	1	1	1	0	Enable 1st rank of DAC1
1	0	1	1	1	0	Enable 1st rank of DAC2
1	1	0	1	1	0	Enable 1st rank of DAC3
1	1	1	0	1	0	Enable 1st rank of DAC4
0	1	1	1	0	1	Load DAC1 (second rank) from first rank
1	0	1	1	0	1	Load DAC2 (second rank) from first rank
1	1	0	1	0	1	Load DAC3 (second rank) from first rank
1	1	1	0	0	1	Load DAC4 (second rank) from first rank
0	0	0	0	0	0	All latches transparent

This device is especially useful in applications where many d/a converters are needed, but space is not available for a large number of IC packages. One such application is in automatic test equipment, where large numbers of DACs are used for waveform generation, level setting, and threshold setting, yet it is

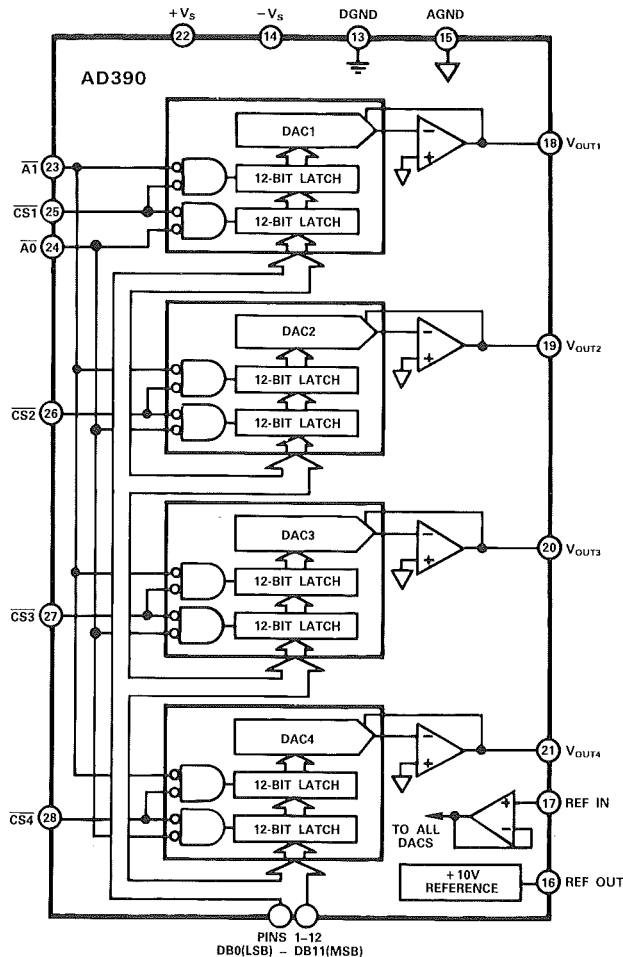


Figure 8.32. 4-channel 12-bit digital-to-analog converter.

desirable to fit the tester in as little floor space as possible. Another application is in automatic calibration of instruments and systems, where the cost of manual adjustment and/or maintenance would be prohibitive.

At the time of publication, no manufacturer of monolithic devices had yet demonstrated the ability to produce a component with functional density and performance comparable to those of the AD390 hybrid. Of course, should this occur, a hybrid manufacturer would be able to use four of these chips in a hybrid.

## 8.6 INTEGRATED-CIRCUIT ADCS

As has been pointed out in an earlier chapter, many circuit techniques have been developed, and several are in widespread use, for converting analog signals to digital form. Of these techniques, the successive-approximation

method has become the preferred approach for performing this function in general-purpose applications, owing to its reasonable speed and resolution for a given amount of circuit complexity. Figure 8.33 is the block diagram of a successive-approximation converter:

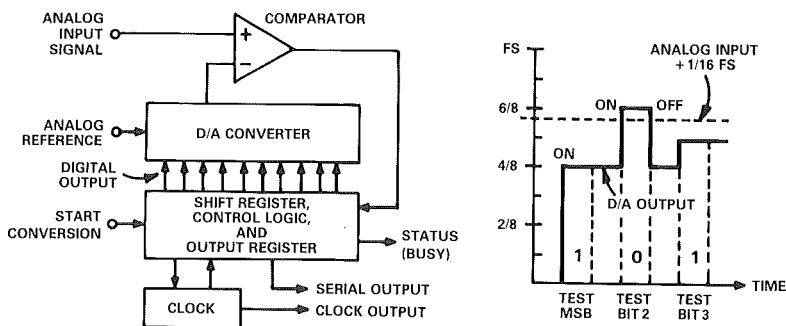


Figure 8.33. Successive-approximation a/d converter.

Both bipolar and CMOS technologies have successfully been employed to produce monolithic d/a converters. The addition of the logic, clock, and comparator blocks to complete the a/d conversion function has been accomplished in both technologies, but—as we shall see—with somewhat different approaches.

### 8.6.1 BIPOLAR PROCESSING WITH $I^2L$

The bipolar process is certainly capable of producing both the DAC and comparator functions. Bipolar technology is also used to fabricate many popular logic families, such as TTL and its derivatives. However, there are significant differences in the processes used for linear bipolar circuits and digital bipolar circuits. For example, bipolar digital circuits are generally designed for relatively low voltage operation (typically 5 volts), and the process is thus tailored for low breakdowns and high speeds. Linear circuits, on the other hand, need a wider supply spread in order to accommodate larger signal swings and achieve reasonable dynamic range. The higher breakdowns generally dictate larger geometries and lower speeds.

Since their objectives seem incompatible, it is therefore difficult to produce both high precision linear circuits and logic functions on the same chip using either the standard linear bipolar or the standard bipolar logic process by itself. A different process must be used.

An approach that has been very successful is the addition of the logic functions to a predominantly linear chip using the integrated-injection logic ( $I^2L$ ) process. This process allows reasonably dense logic to be included on the same chip as high-breakdown precision linear circuitry. This process was used in the production of the AD571 monolithic 10-bit ADC in the late 1970s.

The  $I^2L$  process is particularly useful in manufacturing ADCs because only a single additional diffusion step is required beyond those used in the standard linear process. Furthermore, this diffusion does not interfere with the other steps in the process, so the analog circuitry is unaffected by the addition of the logic. The tradeoff between  $I^2L$  operating current and speed makes conversion times in the 2-3 microsecond-per-bit range possible with manageable amounts of supply current (and thus tolerable power consumption).

Unlike most logic families, the  $I^2L$  family uses multiple fan-out connections (multiple collectors) in a wired-or fashion rather than multiple fan-in connections (multiple emitters). This means that the IC designer must re-think the interconnection concepts, but the basic logic functions are still the same (Figure 8.34).

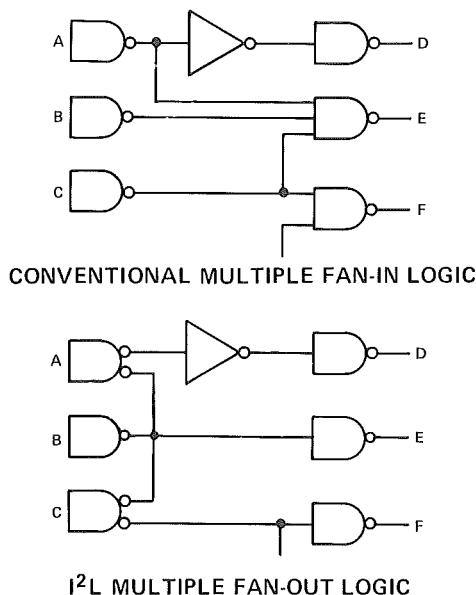
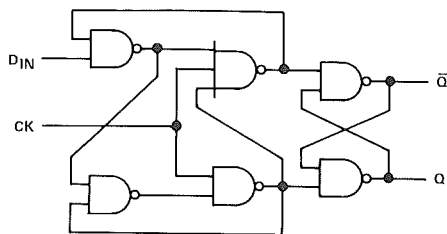
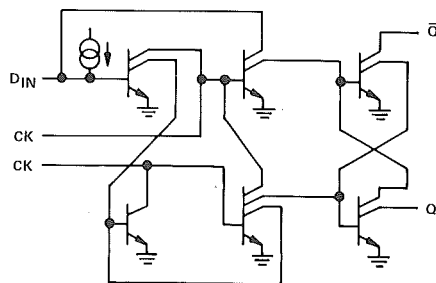
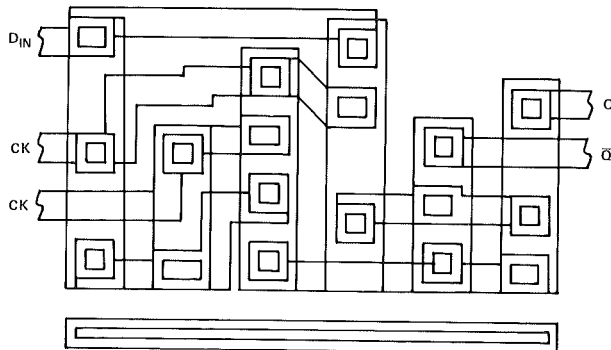


Figure 8.34. Comparing multiple fan-in logic with  $I^2L$ 's multiple fan-out logic.

The simplicity of  $I^2L$  logic compared to conventional TTL logic is amply illustrated with a moderately complex function, such as a D-type flip-flop (Figure 8.35). The equivalent of six NAND gates is required to perform the function—in TTL, the four input gates require three components—two active and one passive—while the two output gates require nine components—five active and four passive—for a total of 30 components (a). The  $I^2L$  flip-flop requires only seven active components, since each multiple-collector transistor is a complete NAND gate (b). The reduction in area is even more impressive because of the simplicity of interconnection (c).  $I^2L$  technology is therefore ideal for implementing a complex logic function such as a successive-approximation register.



a. D-type FF using standard NAND gates.

b. D-type FF using  $I^2L$  gates.c. On-chip  $I^2L$  interconnections.Figure 8.35. Comparison of TTL and  $I^2L$  logic in building a D-type flip-flop.

### 8- and 10-Bit ADCs

The 8-bit AD570 and 10-bit AD571 (Figure 8.36) employ the  $I^2L$  process to perform the SAR function. Each is a completely self-contained converter with internal clock, voltage reference, laser-trimmed DAC, and three-state output buffers. No external components are required to perform a full-accuracy conversion in less than 40 microseconds. The three-state output buffers are open whenever the blank/convert command is in Blank, or during a conversion; immediately after a conversion they come on and present data.

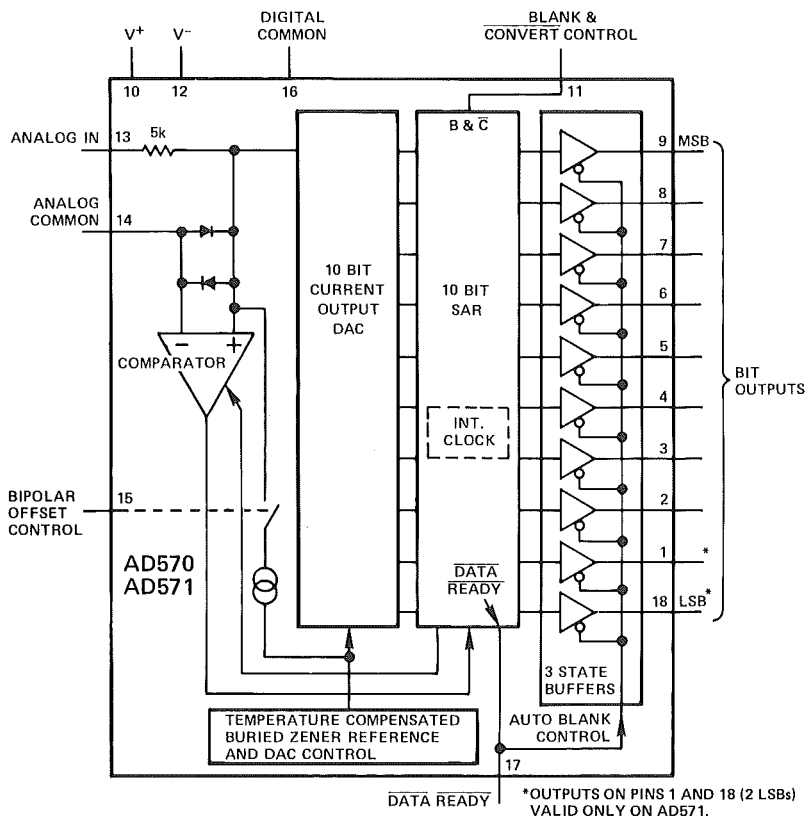


Figure 8.36. AD570/AD571 8/10-bit a/d converter with automatic 3-state outputs for single-line control.

The AD570 and AD571 are well-suited to applications where direct bus interface is not required. Where needed, the newer 10-bit AD573 and 8-bit AD673 (Figure 8.37), which use two additional package pins, provide bus-interface capability.

### 12-Bit ADCs

A logical extension of AD571-based technology is into the 12-bit area. But going from 10 bits to 12 bits requires more than adding two more switches, resistors and register states. In order to attain true 12-bit accuracy and stability, larger (and often many more) components must be used in critical locations. For example, trimming a resistor to  $\pm 0.006\%$  ( $\pm 1/4$  LSB at 12 bits) requires larger trim areas than would be necessary to trim to  $\pm 0.24\%$  ( $\pm 1/4$  LSB at 10 bits). Transistors need to have larger geometry for more predictable performance.

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output-buffer circuitry for direct interface to an 8-, 12-, or 16-bit microprocessor bus. The AD574A design is implemented with a

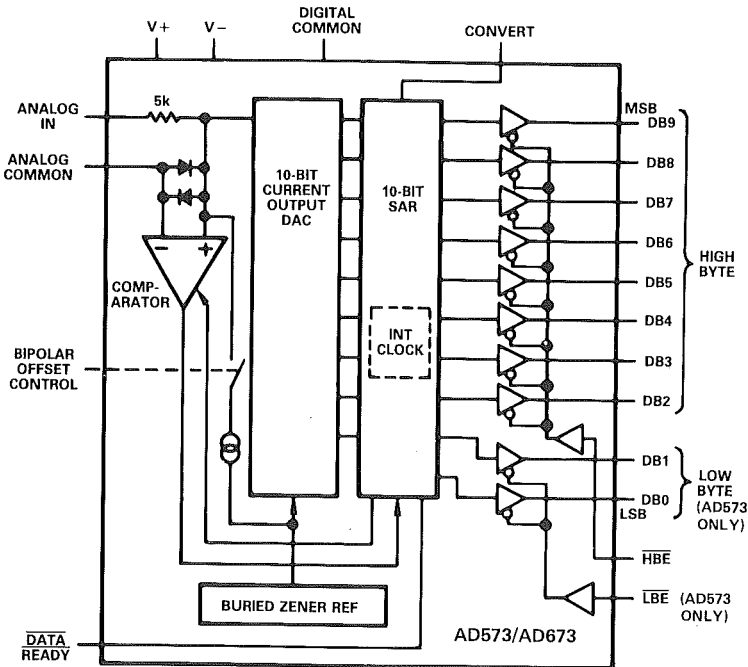


Figure 8.37. Block diagram of 10/8-bit a/d converter, capable of interfacing with 8- or 16-bit buses.

single LSI chip containing both analog and digital circuitry, resulting in maximum performance and flexibility at low cost.

Its introductory form, the AD574, which emerged as the industry-standard 12-bit ADC in the early 1980s, was manufactured using compound monolithic construction, based on two chips—one an AD565 12-bit current-output DAC, including the reference and scaling resistors, and the other containing the successive-approximation register (SAR) and microprocessor-interface logic functions, as well as the precision latching comparator. The block diagram is shown in Figure 8.38.

In 1985, the device became available in monolithic form for the first time; this made low-cost commercial plastic packaging possible. The transition from the two-chip version to the single-chip version was not made until manufacturing yields on the larger single chip reached economically viable levels. In performance, the monolithic version is a direct replacement for the two-chip device. A comparison of the physical appearance of the two devices appears in Figure 8.39.

At the time this is being written, CMOS technology cannot provide either a reference with comparably low drift or a high-speed comparator function. Likewise, bipolar processes without compatible I<sup>2</sup>L are incapable of providing logic which is both fast enough and low enough in power to manufacture a 574-equivalent.





sive-approximation function. Rather than a string of D-type flip-flops connected as a shift register, the AD670 uses a delay line consisting of 80  $I^2L$  gates to establish the timing sequences for the conversion. The delay-line SAR eliminates the need for a well-controlled clock oscillator on the chip. The timing sequence of the conversion is established by generation of a pulse at the beginning of a conversion and its propagation along the delay line, with taps on the delay line at points which allow appropriate timing for register reset, bit trials, DAC settling, and latching of data into the output registers. Figure 8.40 is a block diagram of the AD670.

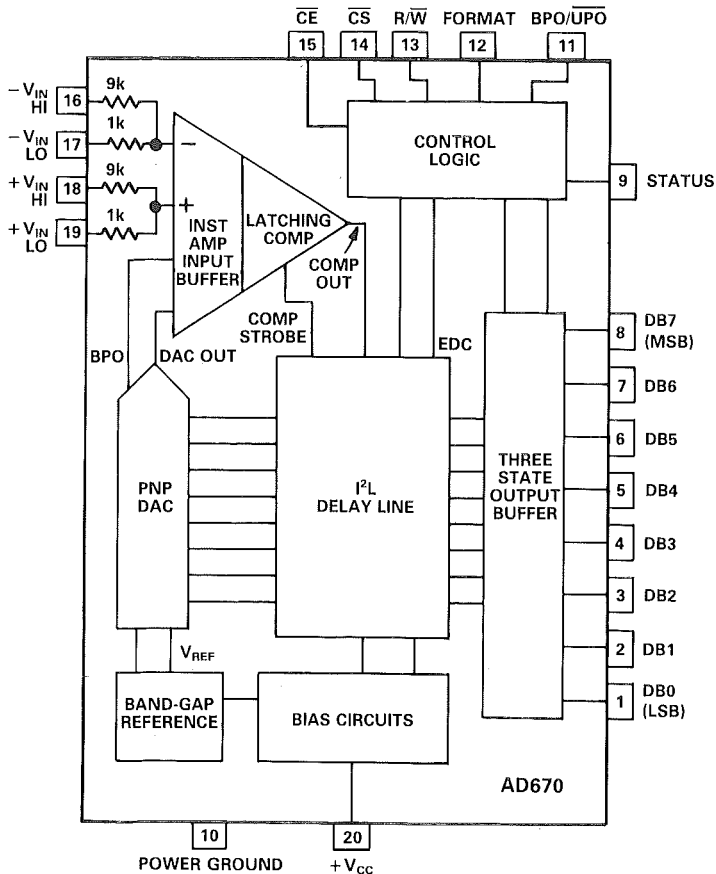


Figure 8.40. Functional block diagram of complete 8-bit ADC, including differential instrumentation-amplifier input.

The 80-gate delay line yields a total conversion time of 8-10 microseconds, fast enough to digitize signals in a wide range of bandwidths. The analog input section includes differential inputs capable of accepting input signals scaled at 1 mV/LSB, yet protected against overvoltages of up to  $\pm 30$  Volts. A precision 10:1 attenuator allows an alternate input range of 2.56 Volts full-scale

(10 mV/LSB). Either unipolar or bipolar inputs are accepted, with output coding software-selectable, as indicated in the table:

BPO/ $\overline{\text{UPO}}$	FORMAT	INPUT RANGE/OUTPUT FORMAT
0	0	Unipolar/Straight Binary
1	0	Bipolar/Offset Binary
0	1	Unipolar/Two's Complement
1	1	Bipolar/Two's Complement

The operation of the AD670 is controlled by the digital inputs  $\overline{\text{CE}}$ ,  $\overline{\text{CS}}$ ,  $\text{R}/\overline{\text{W}}$ ,  $\text{FORMAT}$ , and  $\text{UPO}/\overline{\text{BPO}}$ . Conversions are initiated by writing to the AD670 ( $\overline{\text{CE}}$ ,  $\overline{\text{CS}}$ , and  $\overline{\text{W}}$  active). The states of the  $\text{FORMAT}$  and  $\text{UPO}/\overline{\text{BPO}}$  inputs during the Write operation determine the input range (unipolar or bipolar) and the output digital data format (straight binary or two's complement). When the conversion begins, the  $\text{STATUS}$  line goes high to indicate that a conversion is in progress. The high-to-low transition of the  $\text{STATUS}$  line indicates that the conversion is complete and that data can be read.

The internal design of the AD670 is based on the AD558-type DAC (Figure 8.11). This architecture was chosen for its combination of speed and completeness as well as its ability to operate from a single +5-volt power supply. The circuit's reference is a low-drift bandgap type, chosen primarily for its low-voltage operation. A Zener-type reference would have precluded +5 V operation, since most Zeners produce output voltages higher than 5 Volts and thus would require higher input voltages.

The input stage of the AD670 is a bipolar-input differential buffer amplifier, with high common-mode rejection, even at high frequencies. This allows voltage to be measured in the presence of noisy grounds and dc common-mode offsets, where a single-ended input ADC might require external signal conditioning. Furthermore, many a/d converters in the same speed range as the AD670 require a buffer amplifier between the source and the converter to decouple the converter's changing input impedance during the conversion cycle (see Section 12.1.7). The AD670, however, provides this buffering on-chip, and presents to the source a resistive load of 10 kilohms (or several megohms on the 256-mV range).

The bipolar process is thus useful when the complete converter function is desired on a single chip. However, its versatility is limited by the availability of logic functions which may be required in more exotic (and logic-intensive) conversion algorithms. Although the linear functions (comparators and references) available in the bipolar process have been demonstrated to be superior to their CMOS counterparts, the digital functions are slower than CMOS, for a given power consumption.

Various versions of the bipolar process are also used to produce very high speed converters using the "flash" technique (Chapter 13). The flash a/d con-

verter is implemented by comparing the analog input with voltage levels representing the boundaries of each of the codes. For example, an 8-bit flash converter uses a reference divider with 255 taps to establish comparison points for each of 255 high-speed comparators. In this type of circuit, speed is the most critical parameter for both analog and digital circuits, and power is a secondary concern. Therefore, bipolar processing is the most often used.

The higher-resolution converters using this circuit technique, along with specially developed high-speed fabrication processes, are available with up to 8 bits of resolution and many tens of MHz conversion rates. Present MOS processes do not lend themselves well to the flash conversion technique, since the usual power advantage of CMOS in the switching mode disappears when the circuitry is operating in its linear range most of the time.

### 8.6.2 CMOS A/D CONVERTERS

For lower speeds, however, CMOS converters using the successive-approximation method can be easily produced. The successive-approximation ADC requires logic to implement the SAR function, a DAC, a reference, and a comparator. The digital circuit capabilities of CMOS are well-understood, making the SAR and interface-control functions relatively easy to implement; also, the suitability of CMOS to DAC manufacture was described in some detail earlier in this chapter. The comparator and the reference are the circuit elements which provide the biggest design challenges in CMOS converters.

Most CMOS converters are designed for use with an external reference, since high-performance bipolar Zener and bandgap references are available at low cost and offer lower drift and noise than most CMOS references. Furthermore, there are many applications which call for either external system references or ratiometric conversion, for which an on-chip reference would be superfluous.

Early CMOS ADCs included neither reference nor comparator functions. Newer designs include the comparator function, and future designs, using improved linear-compatible CMOS processes, may include the reference.

#### *8-Bit A/D Converters*

A good example of a successive-approximation converter implemented in CMOS is the Analog Devices AD7574 (Figure 8.41a). It performs an 8-bit conversion in 15 microseconds and interfaces easily to microprocessors, while consuming only a few milliwatts of power.

The comparator used in the AD7574 is designed to resolve LSBs of a few tens of millivolts and is normally used with a 10-volt full-scale range, established by an external  $\pm 10$ -volt reference, e.g., a low-cost bandgap type.

A newer 8-bit ADC, the AD7576 (Figure 8.41b), uses the linear-compatible



Since the strength of CMOS lies in its ability to integrate logic functions, it is not surprising that the AD7576 features several microprocessor interface modes.

- **Timing and Control.** The AD7576 is capable of two basic operating modes which are outlined in the timing diagrams of Figures 8.42 and 8.43. These two operating modes are an asynchronous conversion mode and a synchronous conversion mode. The selection of the required operating mode is determined by the status of the MODE pin. When this pin is HIGH, the device performs conversions only when the required control signals ( $\overline{\text{CS}}$  and  $\overline{\text{RD}}$ ) are applied; with this pin LOW, conversions are performed continuously, and  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  are used only to access the output data.

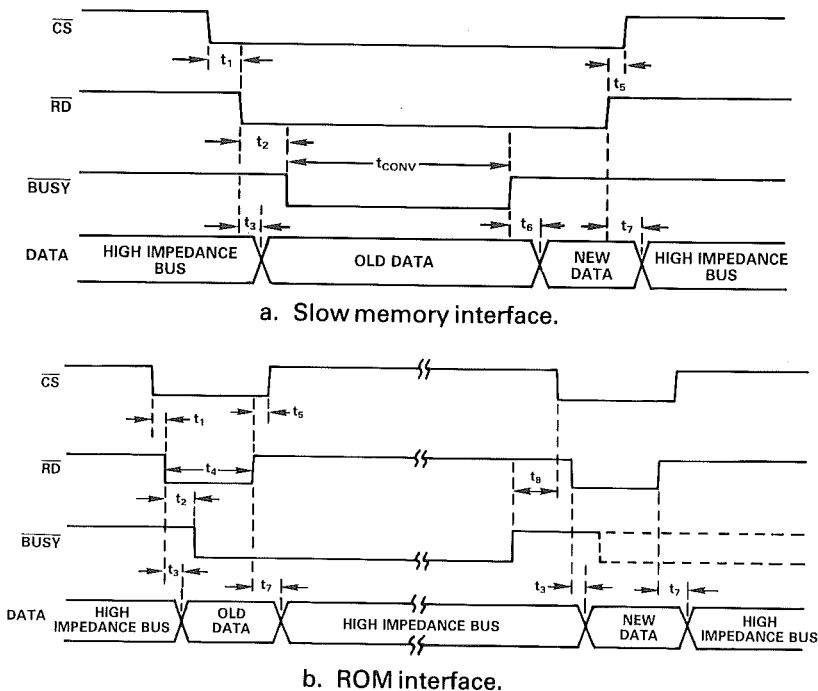


Figure 8.42. Synchronous conversion mode timing diagrams.

- **Synchronous Conversion Mode.** In the synchronous conversion mode (the MODE pin tied HIGH), the AD7576 will perform a conversion when requested to do so by the microprocessor. Once the conversion is performed, two interface options exist for reading the output data from the AD7576.

- **Slow Memory Interface.** The first of these interface options is intended for use with microprocessors which can be forced into a WAIT state for at least 5  $\mu\text{s}$ . The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7576 address.  $\overline{\text{BUSY}}$  subsequently goes LOW, forcing the microprocessor READY input LOW, thus placing the processor

in a WAIT state. When conversion is complete ( $\overline{\text{BUSY}}$  goes HIGH), the processor completes the memory READ. The timing diagram for this interface is shown in Figure 8.42a.

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT, and then READ data with a single READ instruction. The fast conversion time of the AD7576 ensures that the microprocessor is not placed in a WAIT state for an excessive length of time.

Many processors test the condition of the READY input quite soon after the start of an instruction cycle. Therefore, in order for the READY input to be effective in forcing the processor into a WAIT state,  $\overline{\text{BUSY}}$  of the AD7576 must go LOW very early in the cycle.

- **ROM Interface.** An alternative interface option in the synchronous conversion mode avoids placing the microprocessor into a WAIT state. In this interface, conversion is started with the first READ instruction, and a second READ instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 8.42b.

Conversion is initiated by executing a memory READ instruction to the AD7576 address. Data from the previous conversion is also obtained from the AD7576 during this instruction. This is old data; it may be disregarded if not required.  $\overline{\text{BUSY}}$  goes LOW during conversion and returns HIGH when conversion is complete.

The  $\overline{\text{BUSY}}$  line may be used to generate an interrupt to the microprocessor, indicating that conversion is complete. The processor then reads the newly converted data. Alternatively, the processor programming may be timed so that the delay between the Convert Start (first READ instruction) and the data READ (second READ instruction) is at least as great as the AD7576 conversion time. For the AD7576 to operate correctly in the ROM Interface mode, CS and RD should not go low before  $\overline{\text{BUSY}}$  returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if CS and  $\overline{\text{RD}}$  are brought LOW within one external clock period after  $\overline{\text{BUSY}}$  goes HIGH, a second conversion does not occur.

- **Asynchronous Conversion Mode.** When the MODE pin of the AD7576 is tied LOW, the device performs continuous conversions, and the control lines CS and RD are used only to read the data from the converter. The timing diagram for this operating mode is outlined in Figure 8.43.

Data is obtained from the AD7576 by executing a memory READ instruction to its address. The A/D process is completely transparent to the microprocessor and the AD7576 will behave like a ROM. Data may be read at any time, completely independent of the clock. This is especially useful in internal clock applications; the user does not have to worry about synchronizing the clock with the READ line of the microprocessor.

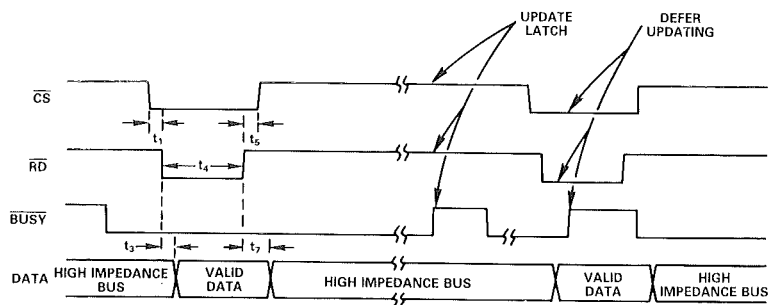


Figure 8.43. Asynchronous conversion-mode timing diagrams.

The data latches are normally updated by  $\overline{BUSY}$  going HIGH. However, if  $\overline{CS}$  and  $\overline{RD}$  are LOW when  $\overline{BUSY}$  goes HIGH, the contents of the data latches are frozen until  $\overline{CS}$  or  $\overline{RD}$  returns HIGH. This ensures that incorrect data cannot be read from the AD7576. The output latches are updated when  $\overline{CS}$  or  $\overline{RD}$  return HIGH and the converter is re-enabled. If  $\overline{CS}$  or  $\overline{RD}$  do not return HIGH the AD7576 will stop performing continuous conversions, and will not start again until either line goes HIGH.

The advantage of this mode is its simplicity. The disadvantage of this mode is that the data which is read is not clearly defined in time; however, it will not be older than one conversion period. If this uncertainty is a problem, it can be overcome by monitoring the  $\overline{BUSY}$  line.

### 12-Bit CMOS A/D Converters

Extension of the performance of CMOS successive-approximation a/d converters to 12 bits and beyond is limited by comparator performance. A significant problem with linear CMOS comparators is that their offsets can be on the order of tens of millivolts; while comparator offset normally produces a simple offset in the converter, it is possible that anomalous behavior (i.e., missing codes) will result if offsets are as large as tens of LSBs in an open-loop circuit like a comparator.

Slower converter types, such as dual- and quad-slope units can tolerate slow response times in their comparators—and/or lower bandwidths (which reduces total noise). Successive-approximation converters, however, need relatively high comparator bandwidths if they are to convert in a reasonable length of time.

A good example of a medium-speed CMOS successive-approximation a/d converter is the AD7582 (Figure 8.44). A four-channel input device, it includes the SAR and microprocessor interface logic, a clock oscillator, and a high-precision autozeroing comparator. It performs 12-bit conversions in 100 microseconds with no missing codes.

The only passive components required are the autozero capacitor,  $C_{AZ}$ , and timing components,  $R_{CLK}$ ,  $C_{CLK1}$  and  $C_{CLK2}$ , for the internal clock oscillator.

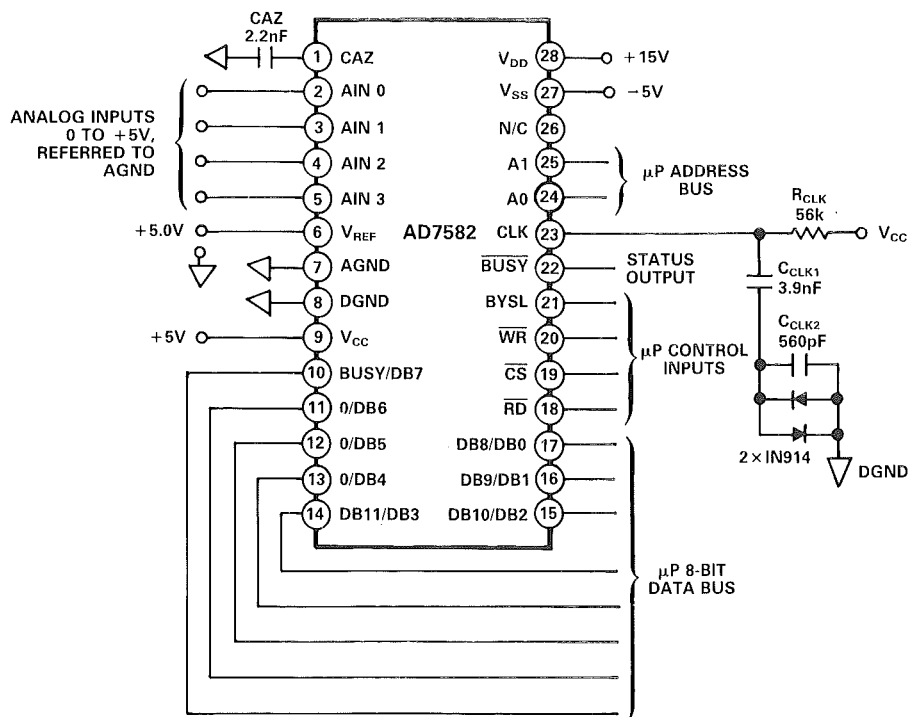


Figure 8.44. Connections to a 12-bit 4-channel CMOS a/d converter.

If the AD7582 is to be used with an external clock source, only  $C_{AZ}$  is required.

Between conversions ( $\overline{BUSY} = \text{HIGH}$ ), the converter is in the autozero cycle. When  $\overline{WR}$  goes LOW (with  $\overline{CS}$  LOW), to start a new conversion, the input multiplexer is switched to the selected channel,  $N$ , via address inputs,  $A_0$ ,  $A_1$ . The autozero capacitor,  $C_{AZ}$ , now charges to  $A_{IN_N} - V_{OS}$ , where  $V_{OS}$  is the input offset voltage of the autozero comparator.

A minimum time of  $10\ \mu\text{s}$  is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for  $\overline{WR}$  to remain LOW for this period of time, since a  $10\text{-}\mu\text{s}$  delay is automatically provided by the AD7582 before conversion actually begins. This is achieved by switching a constant-current load across the clock capacitors, causing the voltage at the  $CLK$  input pin to slowly decay from  $V_{CC}$ . It occurs after  $\overline{WR}$  returns HIGH;  $\overline{WR}$  returning HIGH also latches the multiplexer address inputs,  $A_0$ ,  $A_1$  (see Figure 8.45).

The internal Schmitt-trigger circuit, monitoring the voltage on the  $CLK$  input, ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant-current load across the clock capacitors is removed, allowing them to charge towards  $V_{CC}$  via  $R_{CLK}$ . When the voltage at the  $CLK$  input reaches the HIGH trigger level, the constant-current load is replaced across  $C_{CLK1}$  and  $C_{CLK2}$ . The MSB decision is made when the LOW



trigger level is reached. This cycle repeats 12 times to provide 12 clock pulses for the conversion cycle.

The autozero capacitor should be a low-leakage, low-dielectric-absorption type. To minimize noise pickup, the outside foil of the capacitor should be connected to AGND. The offset voltage of the comparator is reduced to approximately 100 microvolts by the use of this autozero scheme. Input impedance of the four analog input channels is very high, and no buffering is required for source impedances up to 2 kilohms. Full-scale is normally 5.000 volts, established by an external reference, and total error is  $\pm 1$  LSB, relative to this reference.

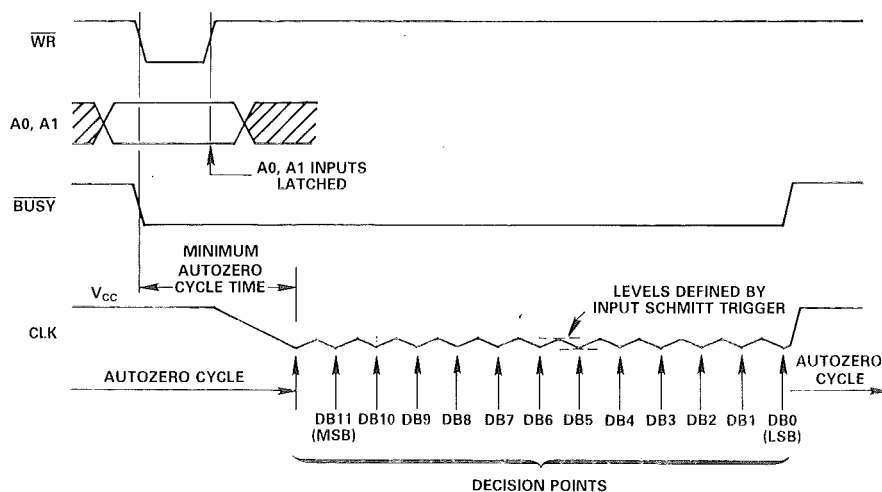


Figure 8.45. Operating waveforms—internal clock of AD7582.

### 8.6.3 HYBRID A/D CONVERTERS

Hybrid manufacturing technology is still quite often used for high-performance a/d conversion. As mentioned earlier, hybrid technology can serve as a means for combining several monolithic device technologies in a small package. Hybrid is particularly useful when the technologies to be combined are normally incompatible and cannot be integrated on a single chip.

An excellent example of the performance achievable with hybrid construction is the AD578 12-bit ADC (Figure 8.46).

The AD578 is a 12-bit successive-approximation a/d converter that uses monolithic devices from incompatible process technologies to obtain optimized performance. For example, the DAC (an AD565) is manufactured using an ion-implanted bipolar linear process—with laser-trimmed thin-film resistors, to provide high linearity; the SAR logic is implemented using high-speed CMOS for high speed at relatively low power; and the comparator is a combination of a standard bipolar device and several discrete devices, to provide fast response from low overdrive, while maintaining low noise and high accuracy.



# Chapter Nine

## I.C. Converter Design Insights

In Chapter 7, “Understanding Converters,” there is a hasty survey of converter design principles. In Chapter 8, there is a discussion of characteristics, architecture, technology, and applications of a representative sampling of popular integrated-circuit converters. The intention of this chapter is to provide more-detailed information on factors the designer must consider in the design and construction of converters for high resolution and accuracy.

Why? In this day and age of monolithic 12-bit converters, it is unlikely (from the standpoint of both cost and engineering effort) that a user would design a converter, except to obtain not-readily available characteristics for a rather special application. Even then, the designer would tend to use available monolithic chips as critical design elements, to which would be added one’s own resources of education and experience. Thus, it should not be our purpose to give our readers a blueprint for constructing a copy of a popular IC converter.

Rather, we are seeking here to create in the reader’s mind—perhaps in somewhat simplified and general form—an understanding of the problems faced by designers of fixed-reference converters employing bipolar transistors, together with some of the answers that have since become classical (and often patented) approaches.<sup>1</sup>

### 9.1 REVIEW OF D/A CONVERTER TECHNIQUES

A current-output d/a converter in effect sums the digitally selected outputs of a set of binary-weighted current sources, as shown in the 6-bit example of

<sup>1</sup>Much of the material for this chapter has been adapted from the monograph, “Circuit Techniques for Monolithic DACs,” (1979), by A. Paul Brokaw, originally published by Analog Devices and now out of print.

Figure 9.1. The DAC consists of a set of six binary-weighted current sources and six switches. The switches are digitally controlled, one switch for each bit. The switches channel the current flow either to the common output summing bus or to ground (in actuality, the grounded line could be used as a complementary output).

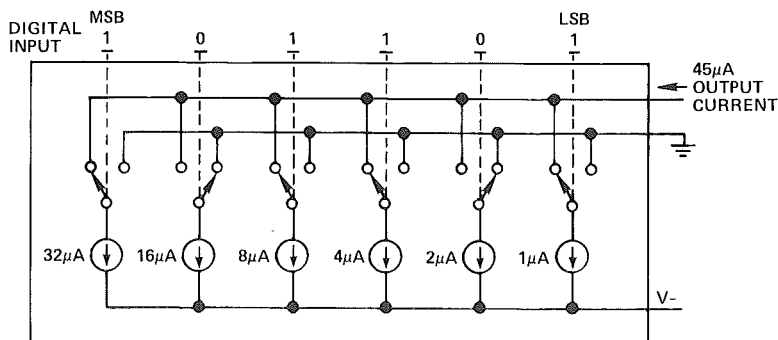


Figure 9.1. Functional schematic diagram of 6-bit current-summing DAC. Digital input 101101 results in  $45\mu\text{A}$  current at output terminal.

The least-significant bit of the digital input (LSB) controls the current source with a weight of  $1\mu\text{A}$  ( $2^0\mu\text{A}$ ). If the bit is 1, as shown, the current is switched to the output line; if the bit is 0, the switch diverts the current to ground, and zero current is added to the output line. Similarly, the second bit controls the  $2\mu\text{A}$  ( $2^1\mu\text{A}$ ) weight by means of the second switch (shown at 0, or off), the third bit controls the  $2^2\mu\text{A}$  current, and so forth.

The current sources are independent, so that the total output current is simply the sum of those currents switched to the output bus. The figure shows the switches responding to the binary code,  $1\ 0\ 1\ 1\ 0\ 1_2 = 45_{10}$  (i.e.,  $32 + 0 + 8 + 4 + 0 + 1$ ), transformed to  $45\mu\text{A}$ . Each of the 64 unique code possibilities maps a binary number into one of 64 possible current values. The code,  $0\ 0\ 0\ 0\ 0\ 0$ , would result in zero output current, and the code,  $1\ 1\ 1\ 1\ 1\ 1_2$ , would result in an output of  $63\mu\text{A}$  ( $64\mu\text{A}$  full-scale minus  $1\mu\text{A}$ ).

Current, in Figure 9.1, is shown flowing from the bus toward the current sources. The choice is arbitrary, but there are two good reasons for having done it that way. First, it is the preferred current direction for the actual structure to be developed, using NPN switching transistors; second, when used with an inverting op amp, to constrain the output bus voltage, this DAC will generate positive output voltage.

### *R-2R Ladder Networks*

Although it is by no means the only method of producing them, the R-2R ladder is one of the most-often used starting points for generating a set of binary currents. Its popularity stems from the fact that although it can be used to

produce currents spanning a range of more than 1000:1, it can be made with only two different resistance values (and even these can be constructed using a single resistance value singly or in pairs). This is an extremely important consideration in an integrated-circuit design, where only a limited range of dependable resistor materials are available in a given circuit. Because of the small range of basic resistivity, resistor values are determined largely by geometry. The range of values is limited on the one hand by photolithographic resolution and on the other by size, in relation to the size of both the chip and the conductors with which a resistor must make contact.

As one might expect, the R-2R ladder consists of a collection of resistors with values  $R$  and  $2R$ . A single-element ladder, driven by excitation voltage,  $E$ , is shown in Figure 9.2. It illustrates that this circuit—which will be developed into a more complex ladder—has a resistance  $2R$ , as viewed from the excitation, and that it divides evenly whatever currents flow into its input ( $2I = E/(2R)$ ) between the leftmost  $2R$  leg ( $I = E/(4R)$ ) and the  $2R$  effective resistance of the remainder of the circuit. Note that this is the same as the resistance which appears at the network input.

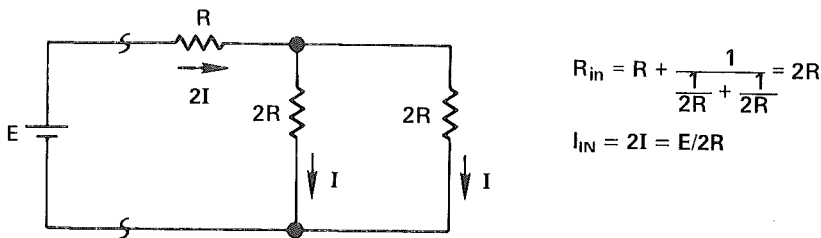


Figure 9.2. Primitive R-2R network. Parallel  $2R$  resistors divide the input current equally; the series combination has a resistance  $2R$ .

Since the resistance is the same, we could add another such network in place of the external  $2R$ , without disturbing the current in the other resistors. Figure 9.3 shows such a circuit. The circuit also looks the same when viewed from the final  $2R$  leg at the right toward the source; however, in order to keep  $I$  in the right-hand resistors constant, the input voltage,  $E$ , must be doubled.

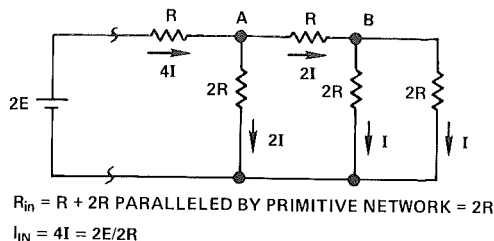


Figure 9.3. Two-stage R-2R network. An additional shunt  $2R$  and series  $R$  cause input currents to divide evenly while preserving input resistance.

With the currents flowing out of node B both equal to  $I$ , the current through the right-hand  $R$  is  $2I$ . Since the currents through the  $2R$  resistances at node A have divided equally, the total current through the left-hand  $R$  is equal to  $4I$ . Thus, the currents through the  $2R$  legs at nodes A and B are related by a factor of 2. The extra  $I$  in the right-hand leg terminating the network is available for further division if additional stages are added. The network can be expanded in either direction. For example, if a shunt  $2R$  is added at the left, a current of  $4I$  will flow in it; a series  $R$  will bring the network resistance back up to  $2R$ , and doubling the input voltage to  $4E$  will permit the same currents to flow throughout the rest of the network.

It should be noted that the voltages at the nodes are also related by factors of 2, since each node is a division point between two equal resistances, equal to  $R$ . Thus, the voltage at node A, in Figure 9.3 is equal to  $2E/2$ , and the voltage at node B is equal to  $2E/4$ . These voltages can be used as the weighting for converters of types other than the ones to be described here.

The expansion process can be repeated as often as we wish by simply adding a parallel  $2R$  resistor and series  $R$  resistor. After each addition, the input resistance of the network will remain unchanged. Each new  $2R$  leg will carry twice the current of the leg to its right. When the network has been expanded to the desired number of  $2R$  branches, it can be driven directly without the need for an additional series resistor, as shown in the generalized  $n$ -leg network in Figure 9.4, where the terminating resistor, at the extreme right, is considered to be an unused zero-order leg.

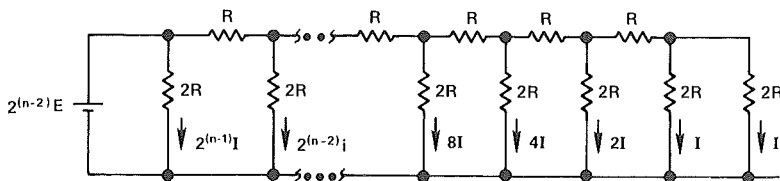


Figure 9.4. An  $n$ -stage  $R$ - $2R$  ladder provides  $n$  binary-weighted currents.

The basic properties of the ideal  $R$ - $2R$  network are that it has a constant impedance, regardless of the number of stages, and that each added stage operates at twice the current (and voltage) of the previous one. This ease of design and expandability, when coupled with its limited requirements on resistance range, further explain its popularity.

### Getting the Currents Out

The network of Figure 9.4 does a fine job of producing binary currents; however, they're all locked up in a closed system. How do we bring them out for use in an application like that shown in Figure 9.1? In Figure 9.4, all the  $2R$  legs are returned to the same voltage, using a common connection. For the network to make the currents available for switching and summation, the re-

sistors must all be returned to the same voltage, *but not necessarily to the same point in the circuit.*

In the circuit of Figure 9.5, the 6-stage ladder is the same, but turned upside down (series legs at the bottom) and driven with negative voltage. The  $2R$  legs have been returned to the emitters of a set of transistors having a common base connection. Neglecting (for now) small differences in base-emitter voltage among the transistors, we can assume that, since the  $V_{BE}$ 's are equal, the network is terminated with approximately the same voltage at the upper end of each leg. As a result, the network will behave as described earlier, producing binary-weighted currents which flow as the emitter currents of the transistors. The collector currents will be slightly less, being reduced by the finite common-base current gain ( $\alpha$ ). Nevertheless, if the transistors are all integrated on the same chip and have the same geometry, we can assume that their  $\alpha$ s match, hence the emitter currents will be reduced in the same proportion at the collector for all transistors, and the collector currents will therefore retain their binary relationship.

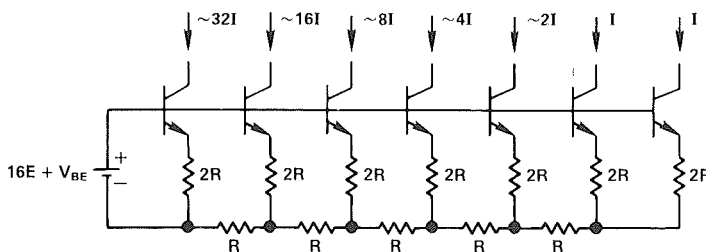


Figure 9.5. Common-base transistors terminate the ladder resistors with (approximately) equal voltages while making the binary weighted currents available as outputs.

Since the excitation voltage must be applied to the common base line instead of directly across the network, the desired excitation must be increased by the expected voltage drop between the common base line and the emitters, i.e.,  $V_{BE}$ .

In practice, this circuit has several weaknesses. They will be discussed shortly. First, let us consider how the currents appearing at the transistor collectors are to be switched off and on and summed.

### Switching

Having shown how the current sources of Figure 9.1 might be developed, we now consider how the switching can be accomplished. One of the most successful approaches is through the Craven cell\*, consisting of a differential NPN current switch controlled by a differential-PNP level translator (Figure 9.6).

\*U.S. Patent 3,961,326

Each of the current sources of Figure 9.5, except the rightmost terminating resistor, will have a switch similar to that shown in Figure 9.6. In the switching element (cell) shown, the lower NPN transistor is one of the current-source transistors; its collector current is one of the binary weighted currents. That current is directed to the common emitters of a pair of NPN transistors, operated so that one of them is normally conducting all the current from the weighting network (on) and the other one is off.

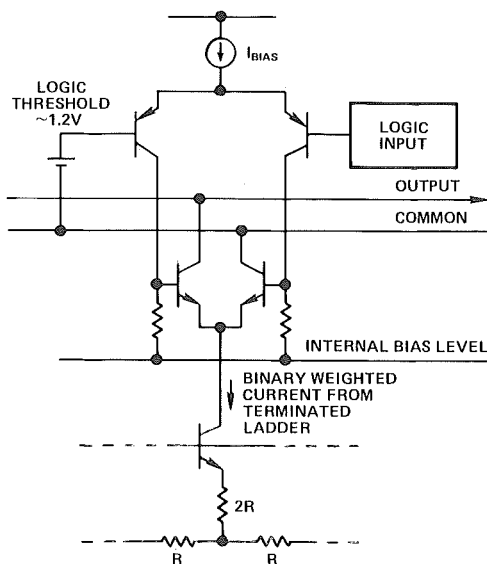


Figure 9.6. Craven cell switches bit-weight current under control of standard logic input.

When the transistor at the left is on, it conveys the weighted current to a line which is connected to all the switches and makes up the output signal, as in Figure 9.1. When the right-hand NPN is on, the ladder current is diverted to another line, which is common to all the switches, generally used as the “ground”—or signal return—line, but sometimes used as a complementary output (i.e., an analog output representing the complement of the digital input word).

The bases of the NPN switches are referred to an internal bias voltage level. Its value is somewhat critical; it must be more negative than the output-line compliance voltage, to avoid saturating the switches, but it must also be more positive than the base line of the current-source transistors, to prevent them from saturating. The NPN pair is switched by driving the base of one of them slightly (300mV to 600mV) positive with respect to the bias rail, while allowing the other base to be held at the bias potential by the associated resistor.

The drive voltage for the bases of the NPNs is generated by a positive bias current, which is controlled by the pair of PNP transistors. One of them is referred to the desired logic threshold (about 1.4V for TTL). The logic signal



is applied to the other PNP. If it is substantially above the threshold, it is to be treated as a logic 1; if substantially less than the threshold, it is treated as a logic 0.

When the input is logic 1, the  $I_{\text{bias}}$  will flow through the left-hand PNP and develop a positive voltage at the base of the corresponding NPN, causing it to carry the current from the current-source transistor to the output bus.

When the input is logic 0,  $I_{\text{bias}}$  will flow through the right-hand PNP and cause it to turn on the right NPN, which will steal the weighted current from the output and direct it to the common "ground", or the complementary output.

In junction-isolated monolithic circuits, the PNP transistors will be lateral structures. Since they are included in the signal path, these reputedly slow devices might normally be expected to severely limit switching speed. In this application, however, they are greatly overdriven and are not required to settle accurately before switching of the NPNs can be completed. Craven cells of this general configuration can be made to switch in 50 to 60 nanoseconds.

### *Output Current Scaling*

The last few figures have shown how binary-weighted currents can be obtained, how they can be made available from the network, and how they can be switched on and off the output bus. Until now, we've skirted the issue of how the excitation voltage can be set and maintained at just the proper level in a monolithic circuit. The problem is made challenging by the requirements to add the base-emitter ( $V_{\text{BE}}$ ) voltage to the excitation voltage (Figure 9.5) and to compensate for the emitter current lost because  $\alpha < 1$ .

In addition it is worth noting that, when the Craven cell is used, the current passes through a second NPN transistor. Even if this transistor were to match the current-source transistor, current from the R-2R ladder is reduced to  $\alpha^2$  of its original value before reaching the output.

The circuit of Figure 9.7 addresses the problem of how the full-scale value of DAC output can be stabilized at a desired predetermined value. We continue to assume that the available output currents are in descending binary ratio, so that if the excitation voltage is set so as to adjust the MSB current to half the full-scale value, the other currents will automatically be at the proper level.

The key to accurate referencing is to use the ability of feedback circuits to compare a parameter (regulated variable) to a desired value and to adjust a related parameter (manipulated variable) electronically until the desired level is equalled.

In the case of the current-output DAC, it is inconvenient to make *direct* measurements of the individual output currents, due to the complications of switching and current summing on the output bus. However, since a series

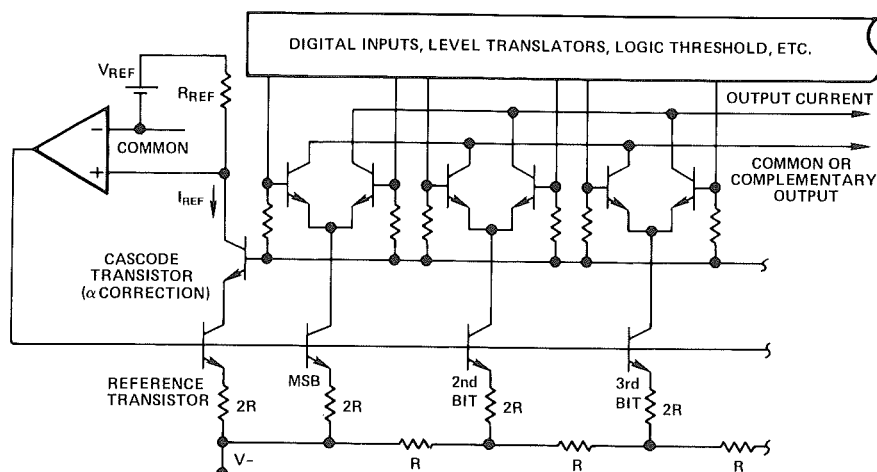


Figure 9.7. Switched-current DAC. Feedback loop precisely quantifies reference current, to which the output currents are ratiometrically matched.

of ratiometrically matched output currents is being produced anyway, very little incremental effort is required to provide an additional reference current, which will track the other currents and provide a representative feedback signal.\* The circuit is arranged so that this current will accurately match the MSB current; and a feedback circuit will be used to adjust the excitation voltage until this reference current is equal to the desired value of the MSB.

In the circuit of Figure 9.7, the R-2R network has an additional 2R section at the left, connected to an additional common-base transistor to form a current source. This resistor-transistor combination is carefully matched to the resistor and transistor used to produce the MSB current. Since the excitation is applied to the two circuits in identical manner, the MSB current will be well-matched to the reference current, whatever the actual value may be.

The output of the reference transistor is passed through a second transistor, which is connected as a cascode and models the switching transistors; the two functions it performs are to insure that the collector of the reference transistor is at very nearly the same voltage as the collectors of the other current sources and to provide compensation for the current loss due to the  $\alpha$  of the transistor that switches the MSB, so that the reference current,  $I_{REF}$ , will match that of the switched MSB.

The amplifier at the left is essentially an inverting op amp; its summing point, held by feedback at nearly 0 volts with respect to common, is at the (+) input because of the voltage inversion inherent at the collector of the reference transistor. The precision voltage,  $V_{REF}$ , and the associated resistor,  $R_{REF}$ , develop a current,  $I_{REF} = V_{REF}/R_{REF}$ , and the amplifier adjusts the base line to whatever voltage is necessary to duplicate  $I_{REF}$  through the collector of the

\*U.S. Patents 3,803,590 and 3,978,473

cascode transistor, irrespective of  $\alpha$ ,  $V_{BE}$ , and their variations with temperature. As long as the MSB current through the switch closely tracks the current through the collector of the cascode transistor, the MSB current will also tend to be equal to  $V_{REF}/R_{REF}$ .

Variation in the initial resistance of the R and 2R resistors is of little consequence, so long as they remain in the proper ratio. This immunity extends to wafer-to-wafer variations due to semiconductor processing, so long as the entire circuit is fabricated uniformly.

Since the driven excitation voltage is the voltage between the base line and the bottom of the R-2R ladder, a viable variation of the circuit of Figure 9.7 is to fix the common base line of the transistors at a constant voltage and drive the bottom of the R-2R ladder from the amplifier output (reversing the inputs to the op amp). This arrangement requires that the amplifier supply the total R-2R ladder current, instead of just the transistor base currents, but it has certain advantages relating to the dynamic performance of the feedback loop, a “plus” with fixed reference and a vital necessity for a multiplying DAC (one that permits a variable  $V_{REF}$ ).

### *Correcting $V_{BE}$ Differences*

By the use of the reference loop, we have corrected significant errors due to  $\alpha$  and voltage drops in the excitation-voltage circuit. A remaining error source, which can be quite significant when good resolution or good multiplying performance is required, is inherent in the differences in base-emitter voltage between the current-source transistors of Figure 9.5.

*The nature of the problem.* For example, suppose that the current-source transistors are all well-matched to one another. Then their base-emitter voltages will differ, since they are operating at different current levels. That is, as we move from left to right in Figure 9.5, each transistor ideally operates at one-half the current of the one to its left. Since base voltage and collector current are logarithmically related, the transistors will have progressively smaller base-emitter voltages. The difference in the voltages means that the individual legs of the ladder do not terminate at the same voltage, and our analysis of the ladder breaks down. The output currents will not be in an exact binary ratio, and the DAC will have errors determined by the ratio of the offset voltage between the emitters to the voltage across the 2R legs.

It's quite possible to eliminate the offset without being required to examine it in detail. However, a detailed examination will lead to better understanding of the solutions, as well as—in fact—a better understanding of bipolar transistor circuitry—an appropriate tutorial goal for this chapter.

Consider two identical transistors, connected as shown in Figure 9.8, with base drive  $V_{BE1}$  and  $V_{BE2}$  and sufficient positive collector voltage ( $+V$ ) to avoid saturation. We will want to keep tabs on the collector currents and the

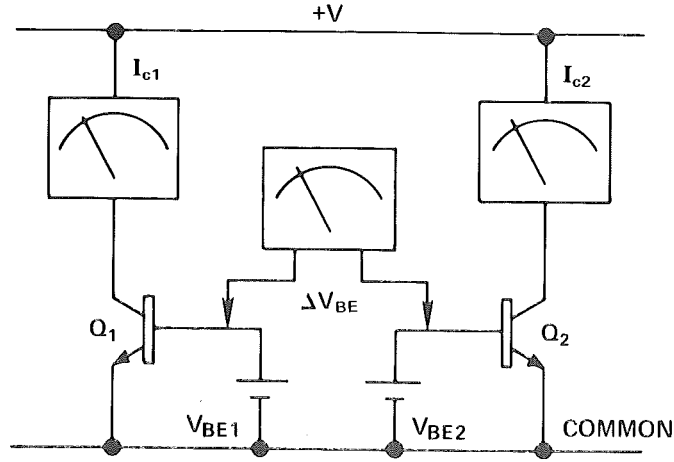


Figure 9.8. Collector currents and base voltages in transistor pairs.

difference in base voltage, symbolized by the meters. The transistors will be assumed to operate in the range of currents described by the relationship,

$$I_c = I_s(e^{qV_{BE}/kT} - 1) \quad (9.1)$$

where  $I_c$  is the collector current,  $V_{BE}$  is the base-emitter voltage,  $I_s$  is the saturation current for a transistor with a particular geometry and doping,  $T$  is absolute temperature, and  $q/k$  is equal to 11,605 kelvins/volt. Inasmuch as an integrated-circuit transistor, operating at—say— $100\mu\text{A}$ , may have a  $V_{BE}$  of about 0.65V at room temperature, where  $q/kT = 39/\text{V}$ , the exponential factor in the equation will be of the order of  $10^{11}$ , and the “ $-1$ ” term is negligible. This simplifies (9.1) to

$$I_c = I_s e^{qV_{BE}/kT} \quad (9.2)$$

Using this approximation, we can readily investigate the effect of operating matched transistors at different currents. If we establish the two collector currents at  $I_{c1}$  and  $I_{c2}$  by adjusting  $V_{BE1}$  and  $V_{BE2}$ , then the ratio of the two currents is

$$\frac{I_{c1}}{I_{c2}} = \frac{I_{s1}}{I_{s2}} \frac{e^{qV_{BE1}/kT}}{e^{qV_{BE2}/kT}} \quad (9.3)$$

Setting  $I_{s1} = I_{s2}$  (since the transistors are matched), and taking the logarithms of both sides

$$\ln(I_{c1}/I_{c2}) = q(V_{BE1} - V_{BE2})/kT \quad (9.4)$$

Hence, the difference between the  $V_{BE}$ 's depends on the log of the current ratio,

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = (kT/q) \ln(I_{c1}/I_{c2}) \quad (9.5)$$

To relate this expression to the problem of Figure 9.5, assume that the currents in the transistors are in a binary sequence. Then the ratio of collector currents in any two adjacent transistors will be 2, and the resulting difference in their base-emitter voltages can be calculated from (9.5) as

$$\Delta V_{BE} = (kT/q) \ln 2 \quad (9.6)$$

which, at room temperature, will be about 18mV. If the fraction obtained by dividing 18mV by the excitation voltage impressed across the R-2R ladder is comparable to the resolution of the DAC, a serious differential-linearity error will result. For example, suppose that the excitation voltage is 6.2V; then 18mV is about 0.003 of full scale, which would be a significant fraction of 1 LSB of 8 bits (for resolution of about 0.004).

In the design of integrated circuits, this error may be avoided or minimized in several ways. The oldest, and still one of the best—from the standpoint of performance—is to equalize the current density in the current-source transistors that terminate the R-2R ladder.

*The multiple-emitter approach.* In the equations associated with Figure 9.8 the transistors are assumed to be of equal area, so that the ratio,  $I_{s2}/I_{s1}$ , is equal to unity. If one of the transistors is larger than the other, this will not be so. For example, if Q2 has twice the emitter area of Q1, then it will have twice the saturation current ( $I_{s2} = 2I_{s1}$ ), and equation 9.5 changes to

$$\Delta V_{BE} = (kT/q) \ln(2I_{c1}/I_{c2}) \quad (9.7)$$

If the currents are in a binary relationship, i.e.,  $I_{c2} = 2I_{c1}$ , then  $\Delta V_{BE}$  will be zero. This suggests that we can eliminate the difference between the emitter voltages of each pair of adjacent transistors by making the transistor with the greater current have a larger area.

It may be simpler to think in terms of passing current  $I$  through one transistor and sharing the  $2I$  current in two parallel transistors. Assuming that the transistors all match, each of the parallel transistors will carry a current equal to  $I$ , and their base-emitter voltages will all be equal. Since the bases are common, the emitter of the transistor carrying  $I$  will be at the same potential as that of the pair sharing  $2I$ , and these legs of the ladder will be properly termi-

nated. Continuing in this way, the next leg, carrying current  $4I$ , should be terminated in four parallel transistors, each operating at a current  $I$ , and so on.

In the transistors used for integrated circuits, extra emitters can be embedded in an enlarged base region. If these emitters are connected in parallel, the base, collector, and multiple emitters of the resulting device will behave like complete transistors in parallel. Figure 9.9 is a cut-away view of a typical integrated-circuit transistor made with four minimum-sized emitters. These emitters can be paralleled by the aluminum intraconnect to yield a transistor with a saturation current which is four times that of a single-emitter device. At a given  $V_{BE}$ , this device will yield four times the collector current of a single-emitter device.

Figure 9.10 illustrates the use of multiple emitters to obtain equal current density, and therefore equal base-emitter voltage, in the transistors terminat-

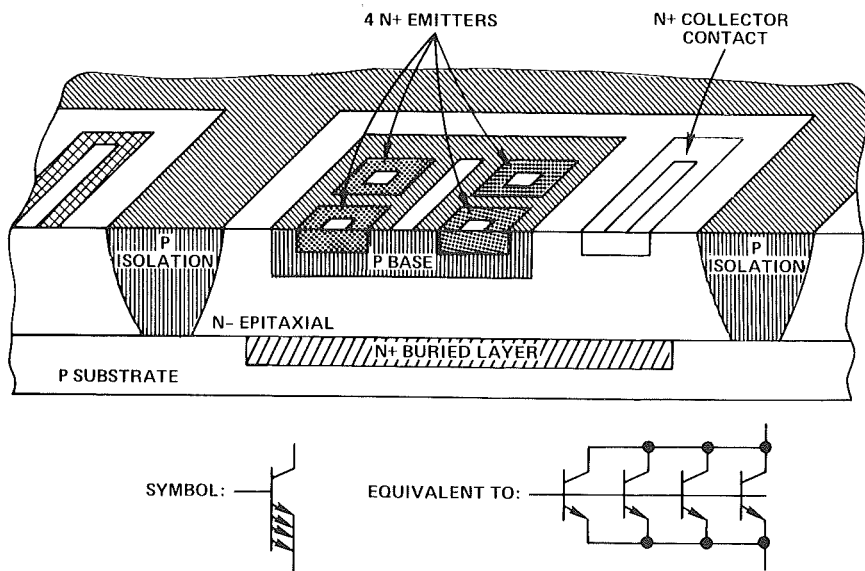


Figure 9.9. Junction-isolated NPN transistor with multiple emitter sites.

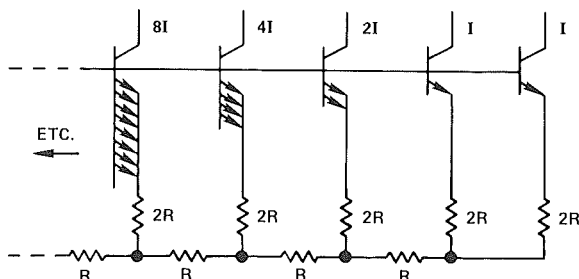


Figure 9.10. Equalizing current density equalizes emitter voltages.

ing a ladder. In the right-hand transistor, each emitter carries a unit of current. In the next transistor, two emitters share two units. In the following transistors, 4 emitters share 4 units of current, 8 emitters share 8 units, etc.

It's that "etc." that brings out the trouble with this solution. For example, in a 12-bit DAC, the weight of the MSB is 2,048 times that of the LSB. This means that the emitter area of the MSB transistor must be more than 2,000 times as large as that of the LSB transistor. Since the minimum emitter size is limited by photolithography, the large device will be very large indeed! This single transistor would be larger than many complete monolithic circuits. Moreover, although the other weighting network transistors would be *smaller*, they would not be *small*.

As a result of this problem, solutions involving current-density equalization by multiple emitters are not often used for DACs having more than 4 or 5 bits. A common practice is to divide a high-resolution DAC into quads (4-bit DACs)\* and then combine their outputs with a second weighting network. For example, a 12-bit DAC function can be realized by making three DACs of 4 bits each and properly combining their output currents in a weighting network.

This solution is shown in simplified form in Figure 9.11. The DAC on the left supplies the four most-significant bits. The DAC in the middle supplies the next four bits. Its actual full-scale output is the same as that of the first four bits. To reduce the weight of these bits in the final output signal, the current is attenuated by a factor of 16. Similarly, the right-hand DAC controls the four least-significant bits. In order for them to have the proper weight in the overall current, the output of this four-bit DAC is attenuated 256 times.

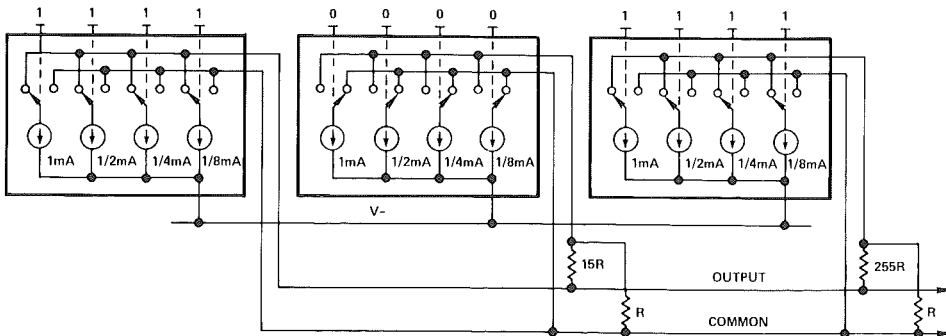


Figure 9.11. 12-bit DAC comprising 3 DACs of 4 bits each plus inter-quad dividers.

With the switches as shown, the current available at the output will be:

$$I_{OUT} = (1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}) \text{ mA} + (\frac{1}{16})(0) + (\frac{1}{256})(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}) \text{ mA} = 1.8823 \text{ mA}.$$

\*U.S. patent Re.31850.

This is equivalent to

$$I_{OUT} = \frac{111100001111_2}{111111111111_2 + 1} \times 2\text{mA}$$

where 2 mA is the full-scale output of the DAC.

To avoid the 255:1 resistance ratio shown, the current in the right-hand DAC may be attenuated by a factor of 16, combined with the current from the middle DAC, attenuated again by 16, and combined with the output of the first DAC. The “interquad dividers,” which mix the outputs of the three DACs in proper proportion, cause the DAC to have a relatively low output resistance. This may be advantageous in high-speed applications, but it requires the output to operate “shorted” (i.e., near ground potential) to obtain the full output current. This may be done by driving the virtual ground at the input of an inverting op amp. Such arrangements are common when the output from such a DAC is to be converted to voltage. The output common bus carries the surplus current from the lower-order DACs and may not be used as a complementary output.

Despite these limitations, the scheme shown in Figure 9.11 is capable of great accuracy and is probably the most widely used basis for high-resolution DACs made with bipolar monolithic and hybrid technologies.

There are several other methods used by designers of precision monolithic converters to equalize the emitter voltages of the transistors used to terminate the binary weighting network. Some of them involve other types of cascades of multiple-emitter transistors in arrangements which permit cycling of the 1, 2, 4, 8 area buildup, in ways comparable to Figure 9.11.

*Offsetting the base voltages.* A method which avoids these complications relies on the fact that the difference between base-emitter voltages of two matched transistors depends on the ratio of collector currents. This means that, in an array of matched transistors (of equal area) operating at currents in a binary sequence, the difference in base-emitter voltage is the same between any two adjacent transistors, as equation 9.6 demonstrates.

This suggests the possibility of driving the bases from a string of equal resistors carrying an appropriate value of current such that there are equal voltage increments between the bases to compensate for the  $V_{BE}$  voltage reduction with decreasing current. However, there is a problem: the  $\Delta V_{BE}$  is proportional to temperature; therefore the correction voltage must also be proportional to temperature.

As a means of developing the correction, consider the circuit of Figure 9.12. It consists of a current mirror comprising a pair of PNP transistors, a pair of NPN transistors with a 2:1 ratio of emitter areas, a control resistance,  $R_M$ , and a measuring resistance,  $R_M/2$ .



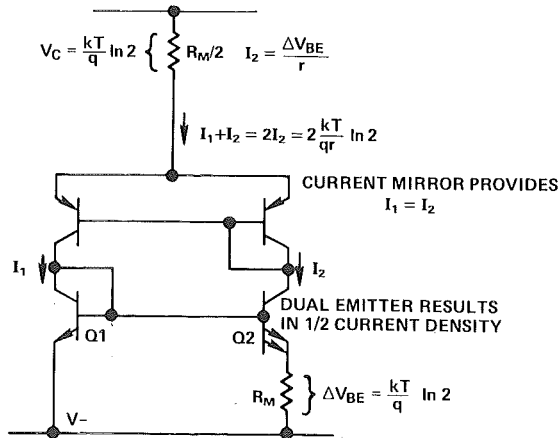


Figure 9.12. Repeater produces a voltage equal to  $\Delta V_{BE}$  at a selected current-density ratio.

The current mirror forces the current in the two sides of the circuit to be equal. Since the two PNP transistors are joined at their bases and emitters, they should have equal collector currents. Neglecting base currents, the collector voltage of Q2 will drive both of the PNP bases to the point that the right-hand transistor absorbs Q2's collector current in its collector. Since the same base voltage is applied to the left-hand PNP, it too will operate at the same current.

Therefore, to a reasonable degree of approximation,  $I_1 = I_2$ , for any value of  $I_2$ . The NPN transistors are similarly connected: their common base connection is driven by the collector of Q1 until Q1 absorbs  $I_1$  at its collector. The resulting base voltage of Q1 is applied to the base of Q2, causing it to conduct the current,  $I_2$ . This arrangement is regenerative at low currents, but the resistance,  $R_M$ , in series with Q2 permits the loop to stabilize as the currents increase and the loop gain drops to unity.

When the circuit reaches its stable condition, we can observe several things. First, to the extent that base current can be neglected, the PNP current mirror should force all four transistors to operate at the same collector current. The emitter current of Q2, which is twice the area of Q1, must divide between two emitters. Since the emitter current of Q2 is approximately equal to that of Q1, the current density is only half that of Q1 in each of the transistors of Q2. Since the transistors of Q1 and Q2 are all matched, the base-emitter voltage of Q2 must be smaller than that of Q1 by an amount

$$\Delta V_{BE} = (kT/q) \ln 2 \quad (9.8)$$

Since the bases are at equal voltage, the voltage difference must appear across the resistor,  $R_M$ . From this, we can calculate the sum of the currents,  $I_1$  and  $I_2$ , in the equilibrium condition.  $I_2$  must be equal to  $\Delta V_{BE}/R_M$ , and, since

$I_1 = I_2$ , the total current flowing through  $R_M/2$  must be equal to  $2I_2$ , and the correction voltage,  $V_c$ , developed across it is equal to  $I_2 R_M$ , or

$$V_c = (kT/q) \ln 2 \quad (9.9)$$

This is the same as the base-emitter voltage difference of matched transistors operating at a 2:1 current ratio, including the temperature proportionality. It has been achieved by generating a current, scaled by  $R_M$ , *proportional to absolute temperature* (PTAT). Circuits of this type are often called “PTAT generators.” An important feature of this circuit is the available voltage compliance; the output of the four-transistor cell is a current which can be made to drive any load which provides more than about 1.5 volts of “headroom” and less than breakdown voltage. This means that the circuit could drive 2, 3, 4, or more resistors in series, and if each had the value  $R_M/2$ , each would independently develop the voltage,  $V_c$ , across itself.

Figure 9.13 shows how a string of series-connected resistors, each producing the correction voltage,  $V_c$ , can be used to equalize emitter voltages.\* In this figure, a few sections of an R-2R ladder are shown with the 2R legs terminated in transistor emitters. The sequence of resistors and transistors is assumed to

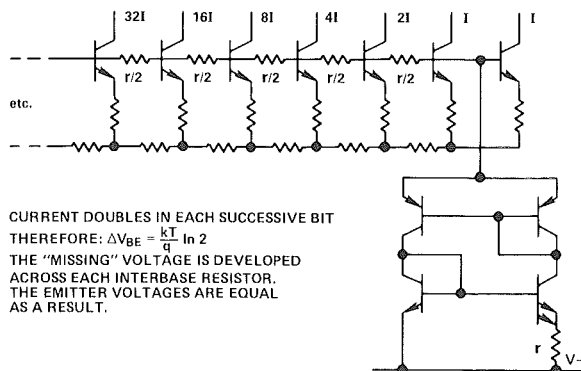


Figure 9.13. Equalizing emitter voltages with PTAT current and ratiometric resistors.

continue toward the left to the desired number of bits, providing very nearly complete correction for the problems mentioned above; and it is assumed to be driven by some suitable excitation circuit, such as the one in Figure 9.7.

Notice that the bases of the transistors are separated by resistances,  $R/2$ . The PTAT generator drives the series string comprising these resistors, and produces a voltage,  $V_c = (kT/q) \ln 2$ , across each of them, as we have seen. Since the base-emitter voltages of adjacent transistors should differ by this same amount, if they produce a binary sequence of currents, the interbase voltages should cause all the emitter voltages to be equal, so that the currents will indeed be in a precisely binary sequence.

\*U.S. patent 3,940,760.

A feature of this scheme that makes it well suited to monolithic designs is that it relies upon ratiometric properties of the circuit elements, rather than upon absolute value. A voltage is produced by essentially the same mechanism which causes the problem. This voltage is then translated to the locations where it can correct the problem by a set of resistors. The absolute resistance values are not at all critical, so long as they have the proper ratio. This requirement is well met by monolithic techniques which may yield variations of as much as  $\pm 30\%$  in initial resistance values, but can reliably produce resistors which match to within a fraction of 1%. Tight ratiometric tolerances can be met by using two  $R_M/2$  resistors in series to form  $R_M$  in the PTAT generator. This and similar techniques are often used to avoid ratiometric errors due to contacting and edge effects in resistors with different geometries (e.g., in the R-2R network itself).

The PTAT generator shown in Figures 9.12 and 9.13 is incomplete, in that it lacks a starter (it also has a stable state in which  $I_1$  and  $I_2$  are zero). This problem is easily solved by providing a small leakage from other bias circuitry in the DAC. This bias can easily be large enough to cause the circuit to regenerate to the desired *on* state and small enough so that it introduces negligible error.

For high-resolution DACs, the elementary circuit of Figure 9.12 has some shortcomings; for example, the effects of base currents were ignored rather than compensated for. However, the principle is valid, and other, more-sophisticated PTAT generators are used in high-resolution converters. This generator was chosen because of the simplicity of illustrating the homomorphism between it and the problem it solves.

## 9.2 APPLYING THE TECHNIQUES TO THE FINAL PRODUCT

The techniques and circuits described here have been used in a number of monolithic converters. One of these converters, the 10-bit AD561, is illustrated in the schematic diagram of Figure 9.14. The R-2R ladder and its terminating resistors are prominent near the center of the circuit. The resistance ladder is terminated after bit 8, and the last two bits and the final LSB termination are produced by using transistors with matched 2:1 area ratios.

In the circuit of Figure 9.14, the base voltage is fixed, and the network excitation is provided by amplifier A2, which drives the resistors. The circuit combines the techniques of Figures 9.9 and 9.13, with multiple-emitter transistors in the three most-significant bits and interbase resistors correcting the remaining error voltages. The interbase resistors are driven by a properly scaled PTAT current with a nominal (room temperature) value of  $120\mu\text{A}$ .

The output of Q1 develops a voltage across a 2,500-ohm resistor between the reference input and the summing point. Amplifier A2 adjusts the ladder voltage to set the current so that the summing point is at zero and the voltage across the 2,500-ohm resistor is equal to the 2.5-V reference. The reference

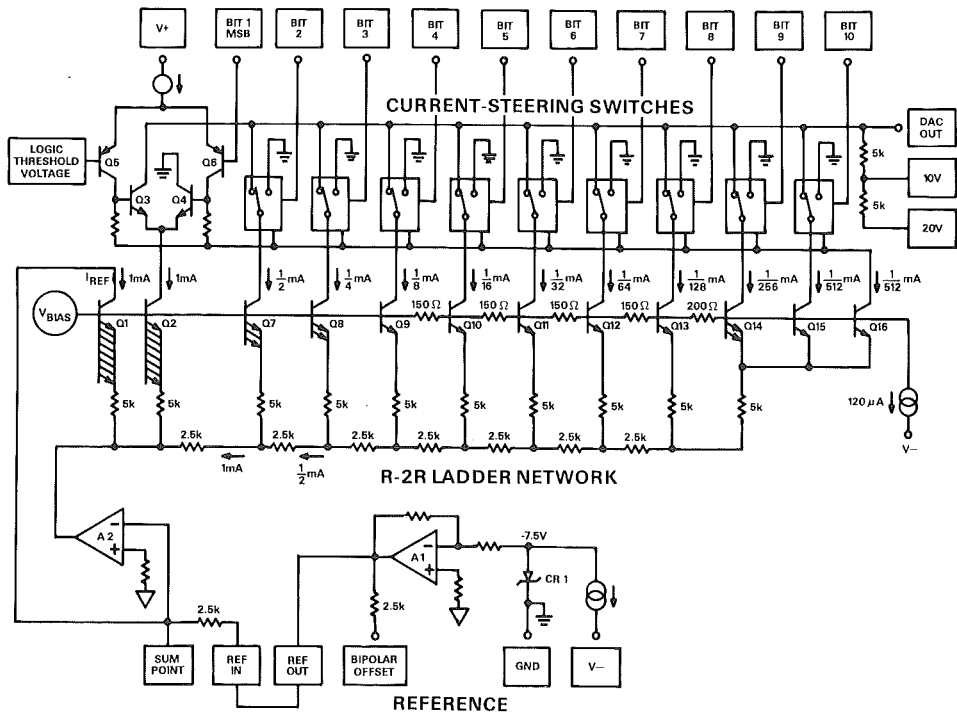


Figure 9.14. Circuit diagram of AD561 10-bit DAC, showing reference, control amplifier, switching cell, R-2R ladder, and bit arrangement.

voltage is generated with a temperature-compensated sub-surface, or “buried,” Zener diode. The amplifier A1 conditions and scales this reference voltage to drive the reference input.

Ten Craven-cell switches are used to control the individual bit output currents. The current-output line also connects to two 5,000-ohm application resistors, ratio-matched to the reference-input resistor, for proper scaling when the DAC is used with an op amp for voltage output.

Since the full-scale output current is determined by the reference voltage and the input resistance, the voltage developed across the applications resistors by the DAC will be in an accurate ratio to the reference voltage. This arrangement ensures that the DAC output depends upon resistance ratios, which can be precisely controlled, rather than absolute resistor values, which are more difficult to control in monolithic circuits.

The full-scale output is, of course, directly related to the absolute value of the reference voltage. Although this voltage is more reproducible than the absolute resistance values, it is still subject to an undesirably wide range of variation in the course of many production runs. To correct this variation, the circuit shown in Figure 9.14 is laser-trimmed at the wafer stage.

### 9.3 LASER WAFER-TRIMMING

Power is applied to the circuit and it is operated via microprobes, and the reference voltage is measured. A fine, high-intensity spot, generated by a laser and steered under electronic control, is used to trim the feedback resistors associated with the reference-voltage buffer-amplifier, A1. These resistors—and many others in the circuit—are SiCr thin-film, deposited on the monolithic chip. The circuit is subjected to *active trimming*, i.e., it is trimmed while functioning, so that the reference-voltage output can be adjusted to its nominal value.

While the wafer is at the laser-trim processing station, other parameters can be adjusted. The temperature compensation for the Zener reference diode is adjusted to minimize the temperature coefficient of the reference-voltage output. In addition, the resistors of the R-2R ladder are adjusted to maximize the accuracy of the DAC. These resistors can be deposited with relatively high ratio accuracy; however the final yield of parts with overall accuracy to 10 bits and better can be substantially improved by laser-trimming.

The use of silicon-chromium thin-film resistors not only permits laser-wafer-trimming; it also ensures improved temperature stability and tracking compared to that obtainable with the commonly used diffused resistor. The temperature coefficient of diffused resistors is of the order of 1600 ppm/°C, which aggravates the ambient temperature sensitivity and—more importantly—results in irreducible errors due to minor temperature gradients on the monolithic chip. On the other hand, the tempco of Si-Cr thin-film resistors is typically less than 50 ppm/°C, with 1 ppm/°C tracking differences.

An interesting problem is encountered when trimming the R-2R ladder. Any of the individual bit currents can be adjusted by trimming its associated resistors. Subsequently, however, trimming *any other resistor in the network* will change the current in the previously trimmed bit. One might wonder if perhaps some interactive procedure could be derived whereby the network is repeatedly trimmed until all bit weights are within satisfactory limits. Fortunately, no such tedious method is required. Instead, there is a straightforward and simple—albeit proprietary—method which requires only one pass through the network and the trimming of no more than half the resistors.

This Chapter has touched on a few of the techniques used to implement bipolar current-summation DACs. Although the current-summation principle is probably the most widely used basis for monolithic DACs (and successive-approximation ADCs, too), it is by no means the only one. It was not our intention to produce here an exhaustive treatise on the various approaches, but rather to illustrate some of the considerations and techniques that have evolved, through the use of a representative example. Some other converter principles employed by Analog Devices are touched on elsewhere in this

book. There is a burgeoning literature in technical journals, the trade press, and manufacturer publications, describing other aspects of converter design—at Analog Devices and elsewhere. A number of references, which will provide fanout, can be found in the Bibliography.

# Chapter Ten

## Testing Converters

The purpose of this chapter is to illustrate common converter errors and deviations from ideal performance, discuss test principles, and outline schemes—for evaluating converter performance—that can be adapted to both manual and automatic testing.

The methods and test-fixture configurations needed to test DACs and ADCs are influenced by the prospective converter applications, nature and speed of tests to be performed, and skill of persons performing and interpreting the tests. The relative importance of the various converter performance specifications depends on the application; the converter user—unless performing a general evaluation—is more interested in testing parameters which significantly influence system performance than those which have little effect on performance.

These factors influence the choice of converter test-circuit configuration and degree of automation: the purpose of the test, e.g., engineering performance evaluation, incoming inspection, or functional checks only; the desired versatility of the test equipment; required measurement speed; data-reduction and display capability needed; and skill level of people intended to perform the tests.

Simple test fixtures designed to test relatively few converter parameters can be implemented easily and inexpensively. These generally must be operated by relatively skilled persons, and test data obtained usually must be number-crunched to extract meaningful performance information.

Although they are expensive when compared to a lashup of available laboratory equipment, general-purpose automatic testers, such as the Analog Devices

LTS-2000 series, perform tests quickly, can be operated by semi-skilled personnel, and are usually quite versatile—easily programmed, self-calibrating, and capable of providing printouts of test results and test statistics over many devices.

Converter performance parameters that are generally of importance are: calibration accuracy (both absolute and relative to full-scale), linearity (both integral and differential), offset, noise, conversion time, and, in the case of DACs, output-switching-transient *impulse* (amplitude-time product). Also of concern are stability of these parameters with variations in time and temperature.

In testing high-resolution converters, there are a potentially large number of data points to be examined to extract meaningful converter performance information. A 12-bit DAC or ADC, for example, has  $2^{12}$ , or 4,096 possible input/output combinations. Fortunately, by knowing the types of converter errors, or deviations from ideal performance, that are commonly encountered, one can devise tests which permit useful performance data to be gained by investigating significantly fewer than the  $2^n$  possible input/output combinations associated with an n-bit converter. Some of these short-cuts will also be discussed here.

### 10.1. D/A CONVERTER TRANSFER FUNCTION

A digital-to-analog converter converts binary numbers, represented by patterns of 1's and 0's, to discrete analog voltages or currents.

The input/output relationship of a DAC, or its *transfer function*, consists of a set of discrete points, corresponding to the number of digital codes, for which each output voltage is a fraction of a reference quantity. The fraction is determined by how the input binary number is coded. Depending on the way the DAC is configured, the transfer function can be unipolar (outputs having only positive or negative values, but not both) or bipolar (outputs can be either positive or negative). In some cases, the reference quantity is itself an input signal; converters used this way are called multiplying DACs (MDACs).

The transfer function of an ideal unipolar 3-bit DAC is plotted as a set of points in Figure 10.1a.

There are many input coding schemes: Figure 10.1a represents a DAC with the most common and best-known code, *natural binary*. In this case, there is a simple linear correspondence between the input codes and the output voltage levels, which—for an n-bit DAC—can be represented algebraically by the following.

$$V_o = V_{FS} \sum_{i=1}^n (b_i/2^i) \quad (10.1)$$



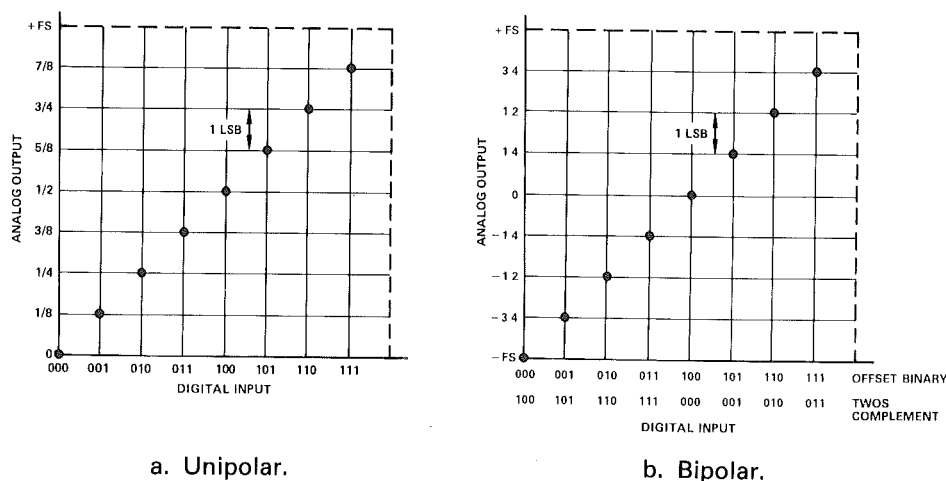


Figure 10.1. Conversion relationships for an ideal 3-bit DAC.

The coefficients,  $b_1 \dots b_n$ , represent the logic levels of the input bits, which can be either 1 or 0.  $V_{FS}$  is the reference quantity, which is usually a simple scalar multiple of the actual input reference voltage (but it does not have to be).  $n$  is the number of input bits: three, in this example.

Coefficient  $b_1$  represents the most-significant bit (MSB), which has a weight of  $\frac{1}{2} V_{FS}$ , and  $b_n$  is the least-significant bit (LSB), which has a weight of  $2^{-n} V_{FS}$  (in this case,  $\frac{1}{8} V_{FS}$ ). Including zero, there are  $2^n$ , or in this case 8, discrete voltage levels, corresponding to the 8 binary codes from 000 to 111.

Looking at equation (10.1), we see that the following conditions apply: (a) with all the input bits set to “0”, the output voltage ( $V_o$ ) is zero, and (b) with all the input bits set to “1”, the all-1’s output (not to be confused with “full-scale” output) voltage is:

$$V_{11} = V_{FS} \left( 1 - \frac{1}{2^n} \right) \quad (10.2)$$

which is one LSB ( $V_{FS}/2^n$ ) less than the full-scale range, or output reference quantity.

These input conditions define the end points of the transfer function; because the relationship is linear, all other points fall on a straight line drawn between them.

Figure 10.1b describes the transfer function of a DAC in the bipolar mode, where the alternate input codings shown are *offset binary* and—with the MSB complemented—the popular *twos complement*.

The bipolar transfer function can be described by the following equation:

$$V_o = -V_{FS} + 2V_{FS} \sum_{i=1}^n (b_i/2^i) \quad (10.3)$$

As in the case of the unipolar DAC, the two measurement end points occur for logic inputs of all “1”s and all “0”s. However, in the bipolar mode, for plus and minus the same value of  $V_{FS}$  (i.e., a *span* of  $2 V_{FS}$ ), an LSB is twice as big as it is in the unipolar mode.

## 10.2 DAC SPECIFICATIONS

The most important specifications of a DAC are *resolution* and *accuracy*.

*Resolution* refers to the number of unique output voltage levels that the DAC is capable of producing. For example, a DAC with a resolution of 12 bits will be capable of producing  $2^{12}$ —or 4,096—different voltages at its output.

Inherent in the specification of resolution, especially for control applications, is the requirement for monotonicity. The output of a *monotonic* converter always changes in the same direction for an increasing digital code. The quantitative measure of monotonicity is the specification of *differential linearity* (step size).

The static absolute *accuracy* of a DAC can be described in terms of three fundamental kinds of errors: *offset errors*, *gain errors*, and *integral (non)linearity*.

Linearity errors are the most important of the three kinds, because in many applications the user can adjust out the offset and gain errors, or compensate for them without difficulty by building end-point auto-calibration into the system design, whereas linearity errors cannot be conveniently or inexpensively nulled out. But before we can understand the nature of linearity errors and how to test for them, the end-point errors must first be established.

### 10.2.1 END-POINT ERRORS

The transfer functions in Figure 10.1 are ideal—hence free from errors. The most commonly specified end-point errors associated with real-world, non-ideal DACs are offset error, gain error, and bipolar zero error:

#### *Offset Error*

Figure 10.2 illustrates the result of offset error only. The actual transfer function is offset from the ideal by two LSBs. Any such error—either positive or negative—that affects all codes by the same amount is an *offset* error.

In most DAC testing, the offset error is measured by applying the zero-scale code (e.g. all “0”s) and measuring the output deviation from 0 volts.

Although it is usually measured at zero, the offset error is not defined as being the error just at zero. It is just that usually no other errors are present at unipolar zero, so determining the offset error is easy. There are some DACs, though (e.g. AD558), where offset errors may be present, but not observable at the zero scale, because of other circuit limitations (such as zero coinciding with single-supply ground) so that a non-zero output at zero code cannot be read

as the offset error. Factors like this make the testing of such devices a little more complicated; it will be discussed in more detail later.

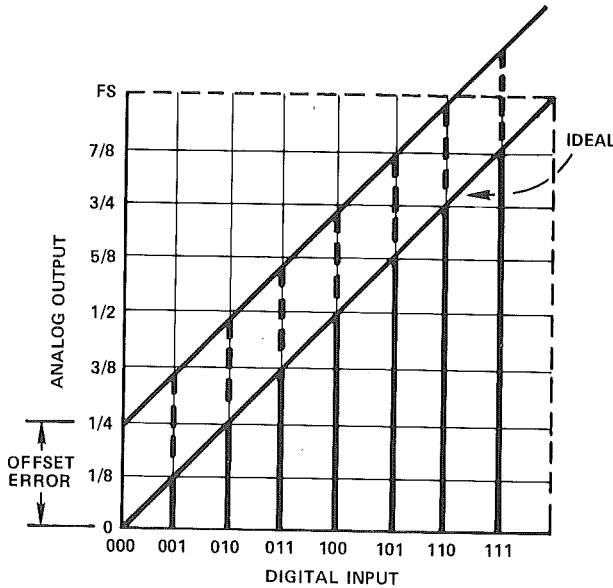


Figure 10.2. An offset error of +2 least-significant bits.

### Gain Error

Figure 10.3 shows the effect of a gain error only. The ideal transfer function has a slope defined by drawing a straight line through the two end points. The slope represents the gain of the transfer function. In real DACs, this slope can differ from the ideal, resulting in a *gain error*—which is usually expressed as a percent because it affects each code by the same percentage.

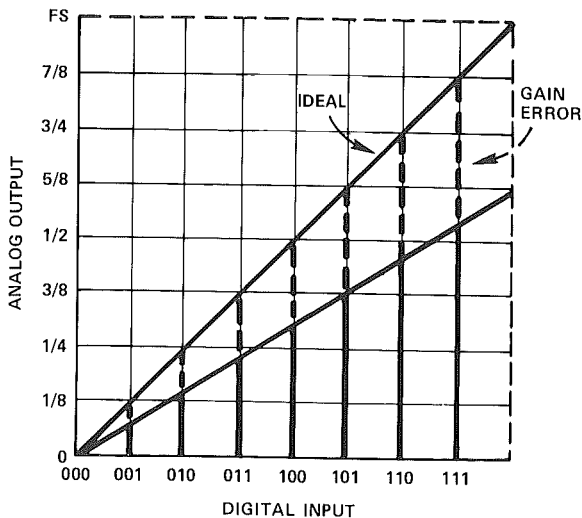


Figure 10.3. A gain error of -37.5%, or 3 least-significant bits at full scale.

Gain error is usually measured by first determining the offset error, then applying all “1”s to the DAC and measuring the error in the all-1’s voltage. Since, by our definition of linearity, that voltage contains only offset and gain errors, the all-“1”s code, which is just 1 LSB less than the *full-scale* (reference) range, is the most convenient code to use to perform measurements to determine gain error.

Gain error is given by:

$$\frac{\text{Error}(\%)}{100\%} = \frac{V_{11} - V_{os}}{V_{FSR}(1 - 2^{-n})} - 1 \quad (10.4)$$

Where  $V_{FSR}$  is the nominal full-scale range (the same as  $V_{FS}$ , for a unipolar DAC),  $V_{os}$  is the measured offset voltage, and  $V_{11}$  is the measured all-“1”s voltage.

### *Bipolar Errors*

In the bipolar mode, the same two end-point errors should be measured. First, bipolar offset error ( $V_{os}$ ), which is usually measured at negative full scale ( $V_{os} = -V_{FSActual} - (-V_{FSNominal})$ ), and bipolar gain error, which is determined by measuring the positive full-scale error and subtracting the bipolar offset error (In Equation (10.4),  $V_{FSR} = 2 V_{FS}$ , and the term “ $V_{os}$ ” is the measured offset,  $-V_{FSActual}$ , which includes any bipolar offset error).

It is also common to specify and measure the *bipolar zero* error because of its importance in many applications. Refer to Figure 10.1b, which shows the ideal bipolar transfer function. The end points lie in the positive and negative regions, but what was mid-scale ( $1/2$ ) in the unipolar mode is now zero scale in the bipolar one. This means that, with the MSB set to a “1”, and all other bits set to “0”, the output should ideally be zero. Any deviation from zero at this code is the *bipolar zero* error. To measure bipolar zero error, apply the code 10 . . . 00 to the DAC (in bipolar mode) and measure the output error from zero.

Bipolar zero error in DACs using offset-type coding is a derived, rather than a fundamental quantity, because it is actually the sum of the bipolar offset error, the bipolar gain error and the MSB linearity error. For this reason, it is important to specify whether this measurement is made before or after offset and gain have been trimmed or taken into account. Because of this error sensitivity, DACs that crucially require small errors at zero are usually unipolar types, with sign-magnitude coding (translated from twos complement, if necessary) and polarity-switched output amplifiers.

## 10.2.2 LINEARITY

### *Definitions*

In a DAC, we are concerned with two measures of the linearity of its transfer function: integral linearity (or relative accuracy) and differential linearity.

Equation (10.1) describes a perfectly linear DAC by both of these measures, since the output is an exact binary-weighted fraction of the reference.

The transfer functions in Figure 10.1 also exhibit the corresponding straight-line relationship between input codes and output voltages. Note that the line has end points at the zero and full-scale voltages. This is consistent with our previous definitions of offset and gain errors and results in an “end-point” linearity specification (i.e., a specification of linearity with offset and gain errors corrected or taken into account). Occasionally, a “best-fit” linearity specification is used (i.e., by adjusting gain and offset arbitrarily to minimize linearity error), but that makes it difficult for a user to determine the actual error budget; fortunately, usage of this specification is becoming rare.

*Relative-accuracy* or *integral-linearity error*, or *integral nonlinearity* (INL), is the maximum deviation, at any point in the transfer function, of the output voltage level from its ideal value—which is on the straight line drawn through zero and full scale.

*Differential-linearity error* (DLE) is the maximum deviation of an actual analog output step, between adjacent input codes, from the ideal step value of  $+1$  LSB (i.e.,  $+V_{FSR}/2^n$ ), calibrated based on the gain of the particular DAC. If the differential linearity error is more negative than  $-1$  LSB (for  $DLE = -1$  LSB, the step is equal to zero), the DAC’s transfer function is non-monotonic.

### 10.2.3 SUPERPOSITION

Before proceeding with illustrations of DAC transfer functions showing linearity errors, it would be useful to consider the property of *superposition* and to be able to recognize its signature. Mathematically, superposition, a property of linear systems, implies that, if the influences of a number of phenomena at a particular point are measured individually, with all other influences at zero as each is asserted, the resulting total, with any number of these influences operating, will always be equal to the arithmetic sum of the individual measurements.

For example, let us assume that the DAC is ideal, except that each bit has a small linearity error associated with it. Equation 10.1 can be rewritten to include these errors, describing the performance of DACs that perform the decoding via a weighted resistor network with  $n$  binary-weighted taps:

$$V_o = V_{ref} \sum_{i=1}^n (b_i/2^i) + \sum_{i=1}^n b_i E_i \quad (10.5)$$

where  $E_1 \dots E_n$  are the linearity errors associated with bits  $b_1 \dots b_n$ .

Equation 10.4 does not apply to equal-resistor networks with  $2^n$  fully decoded taps (segment architecture). In that case, we should write:

$$V_o = V_{\text{REF}} \sum_{i=1}^{2^n-1} (s_i/2^n) + \sum_{i=1}^{2^n-1} (s_i E_i), \quad (10.6)$$

where  $s_i$  is the decoded logic state, 1 or 0, of each segment and  $E_i$  is the linearity error associated with each segment.

Ideally, each bit- or segment error, ( $E_i$ ) is independent; therefore, the linearity error at any code is simply the algebraic sum of the errors of each bit, or segment, in that code (i.e. superposition holds). In addition, by using end-point linearity, we have defined the linearity error in the vicinity of full scale to be zero. Thus, the sum of all the errors must be zero, since all bits, or segments, are summed to give the all-“1”s value.

The errors can be either positive or negative; therefore, if their sum is zero, the sum of the positive errors (positive summation) must be equal to the sum of the negative errors (negative summation). These two summations constitute the worst-case integral-linearity errors of the DAC.

Transfer functions can be drawn for DACs that have linearity errors for which superposition holds. Note that both segment-type and n-tap DACs have transfer functions that are symmetrical about the ideal straight line (Figure 10.4).

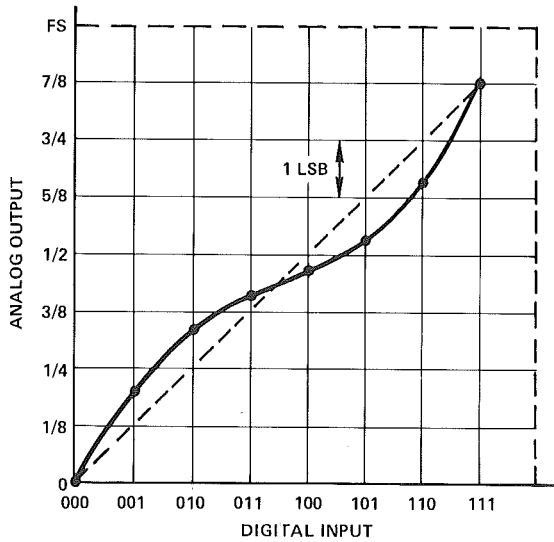
These two figures are significant because they illustrate two different kinds of behavior in the relationship between integral linearity and differential linearity.

In the transfer function of Figure 10.4b, the two codes with the worst-case positive and negative integral linearity errors are adjacent to one another, which results in the worst-case differential linearity error of twice the integral linearity error. This illustrates the consistency of specifying n-tap DACs as having  $\pm 1/2$  LSB INL and  $\pm 1$  LSB DNL. This two-to-one relationship is common for n-bit DAC's built with n binary-weighted circuit elements. Worst-case errors are often at half-scale, due to the sensitivity to element mismatches in that region, and the involvement of all bits in that transition.

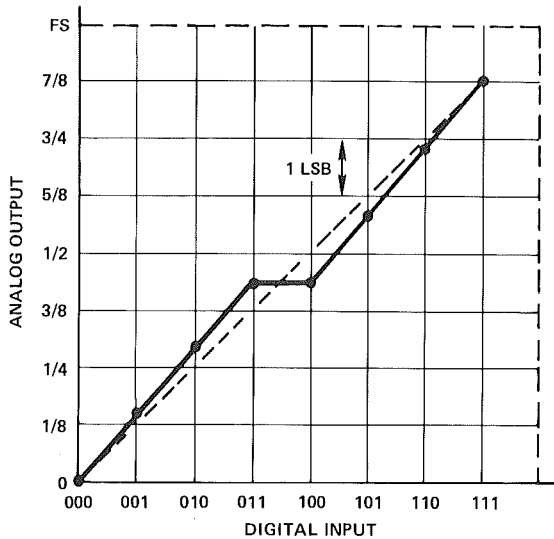
Figure 10.4a, on the other hand, shows a much smoother transfer function, illustrating that the DNL error can be much less than twice the INL error. This relationship is typical of DACs built with “segment” architectures, which are much more tolerant of element mismatches for DNL performance.

For DAC's in which superposition holds, relative accuracy therefore bounds the worst case differential nonlinearity; often, as in the case of segmented architectures, the differential linearity is far better than the relative accuracy predicts for n-tap DACs.

Summarizing, if an n-bit DAC is linear to  $1/2$  LSB of n bits, we are certain that its differential-linearity error is no more than 1 LSB and that the response is monotonic. On the other hand, if the DNL error is less than 1 LSB, we cannot be assured that the DAC is linear to  $1/2$  LSB of n bits.



a. Linearity error of a  $2^n$  decoded DAC, showing large integral linearity errors but low differential nonlinearity.



b. Linearity error of  $n$ -tap encoded-resistor-network DAC. Symmetrical integral linearity error with  $DNL = -2 \times INL$  at major carry, showing DAC on the verge of non-monotonic behavior even though integral linearity is within  $\frac{1}{2}$  LSB.

Figure 10.4. Linearity errors without superposition error.

Having discussed the case of DACs for which superposition holds and for which there is thus no interaction between the bits—or segments—we must now say that completely independent or non-interacting errors is an ideal

which cannot be entirely achieved, unless expensive steps are taken. In most well-designed DACs, reasonable compromises can be made to make the interactions negligible. Occasionally, DAC's appear which have significant interactions, producing non-symmetrical transfer functions like those illustrated in Figures 10.5a and 10.5b.

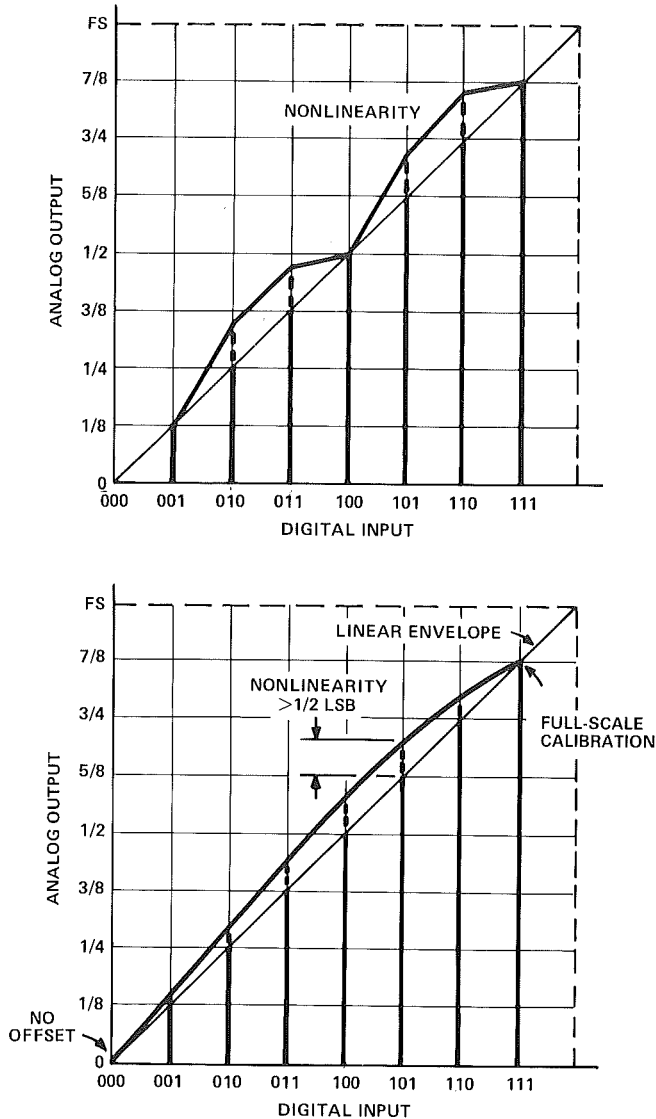


Figure 10.5. Examples of non-symmetrical integral linearity errors due to bit or segment interactions.

These non-symmetrical transfer functions can make testing for linearity errors more complicated, because there are no neat rules, like the one



exemplified in equations 10.5 and 10.6, that make it possible to predict errors from a few sample test points.

### 10.3 DAC TESTING

We are now in a position to begin forming a test strategy for DACs. For characterization or small-quantity testing, there is no substitute for testing all codes and plotting the entire transfer function. Bench instrumentation is available in the form of meters, dc standards, and voltage dividers approaching 1 ppm, or 20 bits of linearity. However, as monolithic technology has evolved to the point that users routinely purchase large quantities of high-resolution and/or -accuracy (12 to 16 bit) DAC's, or evaluate DACs from a large number of possible sources, testing strategies have developed to guarantee performance with the least number of tests, using equipment that is as inexpensive as possible.

#### 10.3.1 STATIC ERRORS

The minimum number of tests required must at least equal the number of unknowns being sought; so an efficient test strategy requires a prior knowledge of the DAC architecture and the degree to which superposition holds.

For example, taking the best possible case, consider an  $n$ -bit DAC built with  $n$  binary-weighted circuit structures and designed with sufficient skill such that bit interactions are negligible. We need to determine: offset error, gain error, and the integral nonlinearity (INL) error of each bit, i.e., a total of  $n + 2$  unknowns. Therefore, we will need to perform at least  $n + 2$  tests.

At the other extreme, an  $n$ -bit DAC built entirely with a "segment" architecture will have  $2^n$  circuit elements with  $2^n$  unknown errors; besides gain and offset error, it will require a maximum of  $2^n$  tests to be sure of finding the worst-case error. In practice, we can take advantage of the fact that the INL changes slowly by design and will find that only a sampling of codes are necessary along the entire transfer function.

A DAC of any architecture with significant bit interactions is even worse than a "segment" DAC, because it cannot be counted on to have a smooth transfer function with slowly changing INL. An all-codes test, or at least an intelligent search routine based on an understanding of the particular bit interactions, will be required.

First, consider the case of a binary-weighted architecture with no bit interactions; what are the optimum  $n + 2$  tests to perform? The measurement of offset error and gain error is straightforward and usually much easier to do than INL, because the offset is measured with respect to ground, and the tolerance on full scale is usually much looser than that on INL.

To determine INL, we could measure the linearity error of each of the  $n$  bits and calculate the positive and negative summation errors to determine worst

case INL. This is an expensive—and often slow—procedure, because a meter with no more than  $\frac{1}{4}$  as much INL as the DAC being tested is required.

### *Major-Carry Technique*

A much better technique, in the case of no bit interactions, is to measure the  $n$  major carries. The three major carries for the 3-bit DAC example would be 001-000, 010-001 and 100-011.

If the DAC were perfectly linear, each carry difference would be exactly one LSB as determined by:

$$\text{LSB} = \frac{(V_{11} - \text{OFFSET})}{(2^n - 1)} \quad (10.7)$$

The errors measured for the major carries can be used to calculate the individual bit errors:

$$\begin{aligned} E_3 &= 001 - 000 - 1 \text{ LSB} \\ E_2 - E_3 &= 010 - 001 - 1 \text{ LSB} \\ E_1 - E_2 - E_3 &= 100 - 011 - 1 \text{ LSB} \end{aligned} \quad (10.8)$$

where  $E_3$ ,  $E_2$  and  $E_1$  are the linearity errors of the LSB, Bit 2 and MSB, respectively. Notice that, since the offset is present equally in each code, it cancels from the calculation; and that any residual gain error, resulting in the wrong ideal LSB calculation, could be eliminated by calculating the sum of  $E_3$ ,  $E_2$  and  $E_1$ , for the total error, and apportioning any difference from zero back to the bit errors in binary fashion.

This is a quite powerful technique, because you can use a null-and-difference circuit with much less accuracy than the DAC being tested. For example, a 1% measuring error in the carry will only produce a 0.01-LSB error in the final INL determination.

This technique is, in fact, being used by manufacturers of sophisticated linear-device automatic test equipment to perform linearity measurements with up to 18 bits accuracy. They build “super DACs,” which are very stable and non-interacting—but not necessarily very linear—and then software-calibrate them, using the major-carry technique.<sup>1,2</sup>

However, most test engineers who have the responsibility for developing DAC test packages for final test, outgoing QC, or incoming inspection, prefer not to assume that the DAC is free from bit interactions; they add linearity

<sup>1</sup>Robert B. Craven and E. Rachel Morris, “An 18-Bit Precision DC Measurement System,” *Digest of Papers*, 1981 IEEE International Test Conference.

<sup>2</sup>Allan Ryan and John Chang, “Versatile System Console for Accurate Measuring,” *Analog Dialogue* 14-3 (1980): 4-5

tests beyond the major carries. This decision is quite often necessary, but it is also expensive because it will require that the test-measurement scheme be significantly more accurate than the DAC being tested.

The most useful tests to add would be to measure the actual linearity errors at the two expected worst-case codes. Recall that if bit interactions are insignificant, these two summation errors will have different signs but equal magnitudes; therefore, the sum of these two errors can be used to estimate the degree to which superposition actually holds. In other words, if the sum of the positive and negative summation errors is significantly different from zero, additional tests will be needed to find the true worst-case INL error.

The most common method for determining the summation errors in non-segment DACs is to measure the INL error of each individual bit, then exercise (and measure) the code that contains only bits with positive errors, and then the code that contains only bits with negative errors. For example, if bits 1, 3, 5, 7 had positive errors, and bits 2, 4, 6, 8 had negative errors, the first code would be 10101010, and the second would be 01010101. This is more accurate than actually adding up the bit errors algebraically, because it avoids the accumulation of up to  $n - 1$  measurement errors.

Measurement of INL errors is easily performed with an accurate, integrating-type voltmeter, but generally such meters perform their measurements too slowly for the accuracy required in testing DACs with resolutions of 10 bits and more. Another problem with purchasing such a meter for converter testing alone is the relatively high cost (for just the meter), compared to dedicated, customized measurement systems present in most of today's automatic test equipment. Finally, an instrument's ability to interface with intelligent controllers affects flexibility and—again—speed.

One of the most popular methods for testing DACs uses a precise reference DAC (REF DAC)—with much higher resolution and accuracy than the DAC being tested—and a differencing circuit (using an op amp or instrumentation amplifier) to provide a measure of the error between the device under test and the REF DAC. Often, the error voltage is amplified (between 10 to 100 times) and applied to the vertical input of an oscilloscope, a chart recorder or the DC voltmeter in an automatic test system. The advantage of the differencing method is that it relaxes the accuracy requirement on the circuit that actually senses the measurement.

### *Bit-Scan Testing*

Figure 10.6 shows the REF DAC technique implemented in a dynamic “bit scan” bench set-up for a 12-bit DAC, with the errors displayed on an oscilloscope. The control logic sequences through all-ones, then each bit individually, then zero, while the comparator and the shift register identify all bit with positive errors to determine which code has the worst-case positive error, and

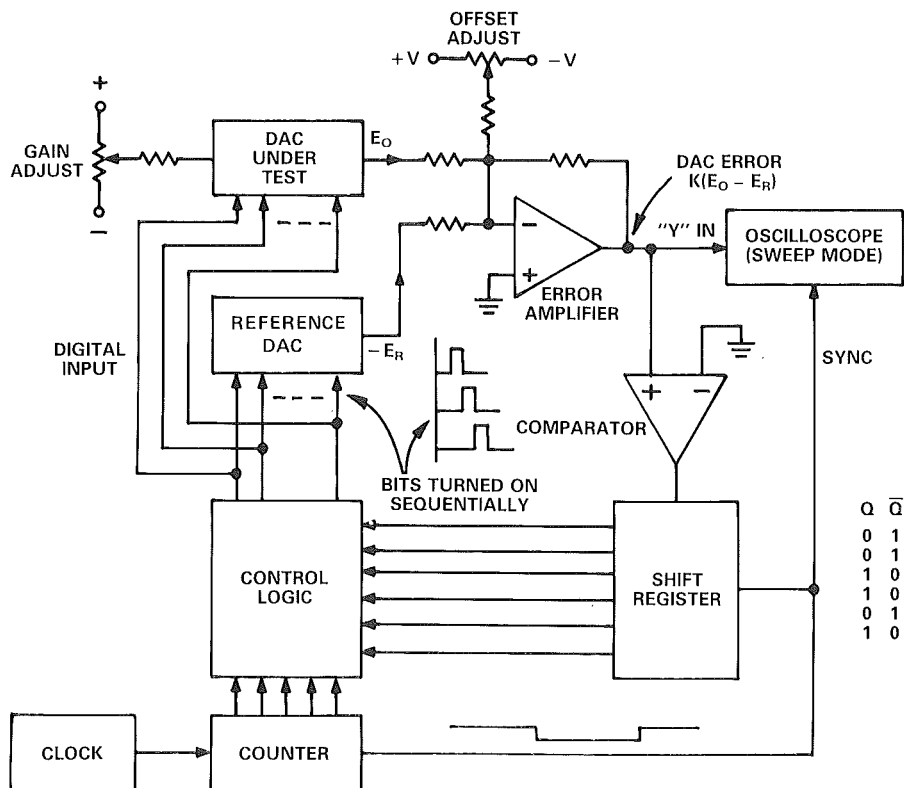


Figure 10.6. DAC dynamic test—bit-scan mode.

all bits with negative errors, to determine which code has the worst-case negative error; then these codes are tested.

Figure 10.7a shows a typical time-slot allocation for testing a 12-bit DAC in this mode. Typical error displays resulting from this test are shown in b, c and d. Figure 10.7b illustrates an error display for a DAC having the correct binary scaling weights for all bits, but full-scale gain calibration 1 LSB high. Since a 1-LSB full-scale gain error (with correct relative scaling) causes the MSB error to be  $\frac{1}{2}$ -bit high, bit 2 to be  $\frac{1}{4}$ -bit high, bit 3  $\frac{1}{8}$ -bit high, etc., the error display is exponential in shape.

Figure 10.7c illustrates the error display for the case of a  $+\frac{1}{4}$ -LSB offset error, combined with a  $-1$  LSB full-scale gain error, with perfect relative weighting (i.e. linearity). This causes a reversal in fullscale error polarity from that shown in Figure 10.7b. In addition, the  $+\frac{1}{4}$ -bit Offset (zero) error shifts the complete display  $+\frac{1}{4}$  bit from the zero baseline.

To find the linearity errors the device under test (DUT) must be calibrated in the following manner: Zero is adjusted to bring the bar representing the zero error (time slot T13 in Figure 10.7a) to the display baseline. The gain is then adjusted to bring the bar corresponding to fullscale (time slot T0) to to

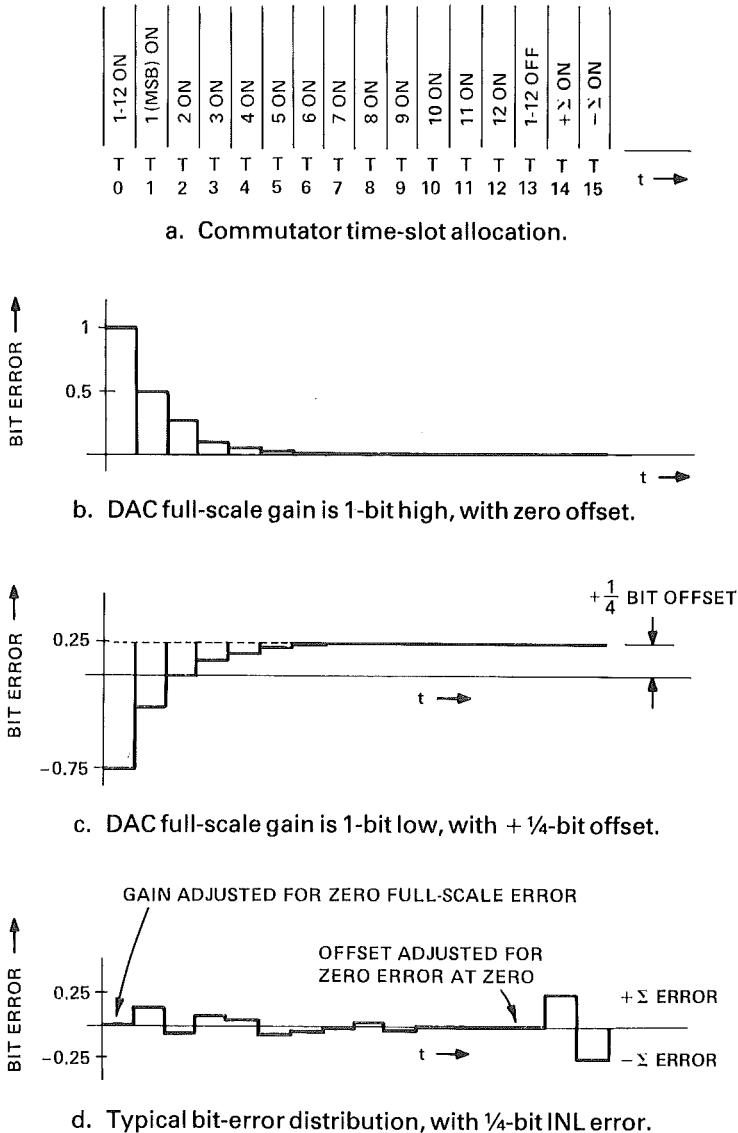


Figure 10.7. Dynamic test waveforms of 12-bit DAC in bit-scan mode.

baseline. Zero and full scale of the DUT are now calibrated. (If the DUT does not have zero or full-scale adjustments, zero and full scale of the reference DAC can be adjusted instead, to normalize the display.)

A typical “bit-scan error” display after zero and full scale of the DUT (or reference DAC) have been calibrated, is shown in Figure 10.7d. If the DUT’s bit interactions are negligible, the sum of all positive bit errors should equal the sum of all negative bit errors after zero and fullscale calibration; any difference indicates the presence of interactions.

A circuit similar to that in Figure 10.6 is found in many automatic test systems, capable of measuring nonlinearities up to 14 bits. In a typical automatic test-equipment (ATE) application, calibration of the circuit's errors, excluding the DUT, would normally be provided for in software. This would include measurement of the error amplifier's offset- and gain errors, caused by mismatches of the amplifier's input-transistor base-emitter voltages & bias currents and mismatches in the feedback- and input resistors.

If an instrumentation amplifier is used instead of an op amp, there would be separate high-impedance inputs for the DUT output and the reference-DAC output and a saving of components. With an instrumentation amplifier, it's wise to measure its common-mode rejection, because it can be significant for DACs having resolutions of 12 bits and more (at 6 dB per bit, a 12-bit DAC would require at least 90 dB of CMRR). The reference DAC may also be calibrated by the system; this amounts to measuring its offset and gain errors (and sometimes the linearity errors, using the major carry technique), and storing them for future software correction.

### 10.3.2 DAC SETTling-TIME MEASUREMENT

DAC settling time is a parameter of importance in high-speed applications. Settling time is defined as the time required for the output to approach a final value within the limits of a defined error band, for a step change in input. This fixed error band is generally expressed as a fraction of full scale, typically  $\pm 1/2$  LSB. If the device's step response overshoots or rings, so that the output swings through the defined error band before entering it for the final time\*, the above definition requires that settling time is measured as the time taken for the output to enter the defined error band for the final time.

The above definition of settling time implies that, the greater the output step change, the longer the settling time (a non-overshooting 1-LSB output step change, for example, has settled to within  $\pm 1/2$  LSB when this change has reached only 50% of its final value.)

The accurate measurement of settling time for a high-resolution, high-speed DAC is fraught with practical difficulties. Measurement instrument bandwidth and thermal unbalance effects, coupled with the unavoidable presence of noise, can introduce significant measurement uncertainties when high-speed settling times to within error bands of the order of the order of 0.01% of final value are being measured. It is particularly easy to overlook a "long tail" in which the output continues to change for hundreds of micro seconds due to thermal gradients or dielectric absorption effects. It takes patience and significant analytical skills to develop, and verify the accuracy of, a high speed settling-time measurement setup.

\*"Final time" does not mean just the final time within the time allotted for the measurement; if long tails (due to thermal or dielectric-absorption effects), orders of magnitude longer than the normal settling time, are suspected, the time allotted for the measurement should be long enough to detect their presence.

There are some important distinctions which must be mentioned when discussing speed and settling-time specifications. If the settling-time error band is described as  $\pm \frac{1}{2}$  LSB, a DAC with 10-volt full scale range and 8-bit resolution has an allowable error band of  $\pm 20$  mV, a 10-bit DAC has a  $\pm 5$ -millivolt error band, and a 12-bit DAC  $\pm 1.22$  mV. A given 12-bit DAC is not necessarily a slower design than a given 8-bit device; it is simply required to settle to within a more tightly specified error band.

Some converters settle faster in one direction than the other; if bipolar operation is considered, voltage output in the negative-going direction can settle much more slowly than in the positive direction. The current-output mode (the standard mode for most IC DACs), settles much faster than the voltage mode, since the currents are simply steered one way or the other, and there is no significant capacitance-charging. In the voltage mode, an output op amp is required, adding a delay, and stray capacitances must be charged by an amount corresponding to the voltage change. There are many ways to optimize settling time in the current-output-DAC/fast-op-amp connection; some of these are discussed in Chapter 12.

Settling time is often measured by looking at crossings on a trace that plots the difference between the output waveform and a voltage representing the final value of output—on an LSB-calibrated oscilloscope triggered by the initiation of the DAC input change. There are two major problems here. One is the narrow extent of the final settling voltage range; it calls for a very fast high-gain preamplifier. The other problem is the wide output swing in relation to the small range being depicted on the oscilloscope screen. It must invariably produce saturation until the trace comes into the final-settling window. Saturation of the oscilloscope preamplifier can cause large errors while the oscilloscope recovers; it can be avoided (or at least mitigated) by using a specially designed preamplifier with high gain, wide bandwidth, and controlled output swing that considerably reduces the amount of overdrive to the oscilloscope.

The circuit shown in Figure 10.8 is capable of measuring current-output 12-bit settling times as low as 200 ns. The unity-gain, high-bandwidth buffer formed by Q1-Q3 holds the DAC output voltage at ground while the current changes appear across R1. The pair of source followers, Q4 and Q5, isolate the scope's input capacitance from R1, and the Schottky diodes limit the signal swing into the plug-in to  $\pm 400$  mV, thereby reducing the problem of overload recovery.

When the magnitude of the LSB is in the neighborhood of 1 millivolt or less, detecting settling to beyond 12 bits requires limiting the input voltage excursion to the oscilloscope even further. Several "active clamping" techniques can be employed.<sup>3</sup> A fairly simple technique, not requiring synchronized

<sup>3</sup>Schoenwetter, H.R., "High-Accuracy Settling Time Measurements," *IEEE Transactions on Instrumentation and Measurement*, Vol. IM-32, No. 1, March, 1983.









final value. Next, the delay is shortened, and after the filtering loop has settled, the resulting offset change represents the converter's output change.

The strobe delay time is decreased in increments suitable for the resolution desired until the converter's instantaneous response is outside the desired error window. In the setup described, the generator can produce pulses as short as 1 ns. *The settling time is interpreted as the strobe delay period at which the offset change first becomes larger than the desired error band—typically  $\frac{1}{2}$  LSB.*

Schottky diodes limit the input to the high-resolution comparator to a few hundred millivolts. A clamped mode on that input is formed by two 4-kilohm load resistors, and a voltage ( $V_{\text{CANCEL}}$ ) equal in magnitude but opposite in polarity to the expected final value of the converter's output for a transition of interest. Because the reference voltages to the converter must be very stable, precision power supplies are required.

## 10.4 A/D CONVERTER TESTING

### 10.4.1 ADC TRANSFER FUNCTION

In the ideal transfer function for a 3-bit A/D Converter (ADC), Figure 10.11, the analog input signal is on the horizontal axis and the digital output is on the vertical axis. Note that, unlike a DAC, where there exists a unique analog value for each digital code, the digital output of an ADC is valid over a range of input signals. The quantum of input for a given output code is called the "width" of the code. The ideal width is exactly 1 LSB (least-significant bit), but, in practice, each code-width is different from its neighbors; acceptable performance will typically occur with codes  $\frac{1}{2}$ -LSB to  $1\frac{1}{2}$ -LSB wide.

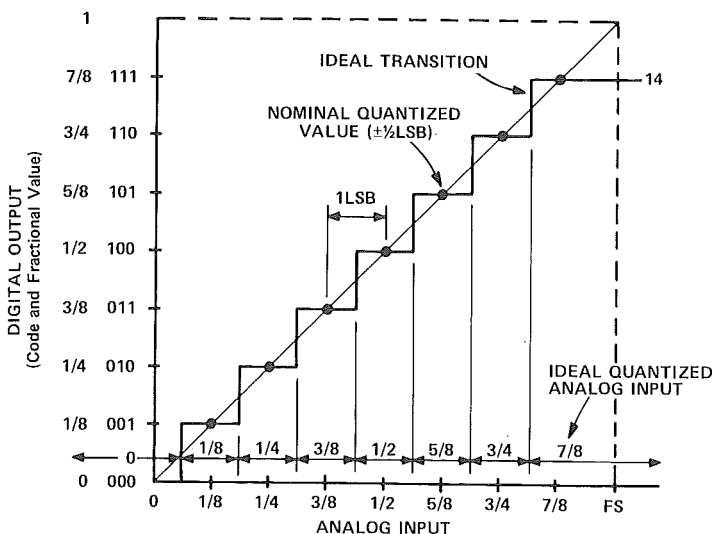


Figure 10.11. Transfer function of an ideal 3-bit ADC.

The transitions between codes occur at unique, measurable input voltages. In ADC architectures which employ a DAC, these transitions ideally occur when the input to the ADC equals one of the discrete DAC output values (comparator and noise can cause them to differ).

Determining the input voltages at which these transitions occur in an ADC is somewhat more difficult than measuring the output of a DAC at a given code. However, once instrumentation for identifying transitions has been implemented, the specifications and testing of ADC transfer functions are similar to those for DACs. That is, similar concepts of gain, offset and linearity apply with equal importance to ADCs.

The ideal analog values at which the transitions should occur in a  $n$ -bit ADC can be calculated as follows:

$$V_{in} = V_{FS} \sum_{i=1}^n (b_i/2^i) + V_{off} \quad (10.9)$$

where  $b_1 \dots b_n$  are the digits of the binary code, starting at the MSB, with values of 0 or 1.  $V_{FS}$  is the reference voltage or full-scale range and  $V_{off}$  is the offset. The analog input voltage,  $V_{in}$ , required to turn on each bit can be found by setting each bit, except the desired one, to zero in Equation 10.9.

Note that Equation 10.9 is identical to Equation 10.1, except for the inclusion of an offset ( $V_{off}$ ) term. The reason for this is that in many ADC's, an offset is intentionally introduced to adjust the positions of the transitions to suit the particular ADC application.

For example, in Figure 10.11, an offset of  $-1/2$  LSB has been introduced, moving the transitions to the left by that amount and aiming the ideal straight line through zero, full-scale range, and the center of each code. Thus, the position of the first transition (from Equation 10.9) is

$$2^{-n}V_{FS} - 1/2 \text{ LSB, or } 1 \text{ LSB} - 1/2 \text{ LSB} = +1/2 \text{ LSB.}$$

#### 10.4.2. ADC GAIN AND OFFSET ERRORS

##### *Unipolar Offset Error*

The transfer function of an ADC is tested for errors in a predictable sequence. The first test to be performed is for offset error. An offset error is defined as a common deviation from the ideal transition voltages. It is usually tested by finding the error of the first (LSB) transition, because it is likely that the offset error is the only significant error present in that transition.

However, to ensure that the offset error is determined accurately, any gain or linearity error of the LSB itself must be subtracted first. To determine any such errors, it is usual to measure the difference in 1-LSB transition voltages between pairs of codes that will yield the actual width of the LSB, for example, code 0 . . . 0100 and code 0 . . . 0101, or some other such combination. The

code-width error, or CWE, is equal to the measured width of an LSB step minus one LSB ( $V_{\text{ref}}/2^n$ ). Once this error is determined, it is subtracted from the first transition voltage; the remaining deviation from the ideal value is the offset error (Figure 10.12). The offset error in the example of Figure 10.12 may be determined by the following equation:

$$V_{\text{off(Err)}} = V_{\text{trans(meas)}} - \text{CWE} - V_{\text{trans(ideal)}} \quad (10.10)$$

where  $V_{\text{trans(meas)}}$  is the actual first transition voltage and  $V_{\text{trans(ideal)}}$  is the ideal first transition voltage. For Figure 10.12, where there are no apparent code-width errors, the offset error in LSBs, calculated from Equation (10.10), is:

$$V_{\text{off(Err)}} = 1 \text{ LSB} - 0 \text{ LSB} - \frac{1}{2} \text{ LSB} = +\frac{1}{2} \text{ LSB} \quad (10.11)$$

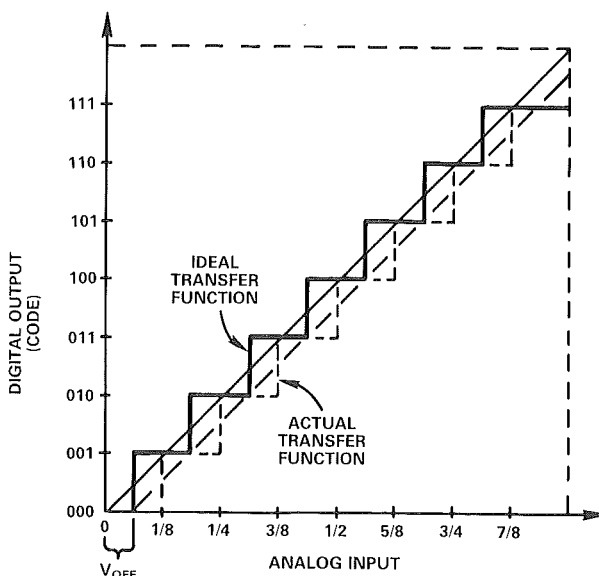


Figure 10.12. Three-bit ADC transfer function with an offset error.

### Unipolar Gain Error

The next test performed is for the gain error. Gain error appears as a change in slope of the transfer function. Thus, gain error is the same as full-scale error, except that the offset error is subtracted. Gain error affects each code in an equal ratio (Figure 10.13).

To determine the gain error of an ADC, measure the final transition voltage and subtract the first transition voltage. Since this interval is ideally equal to  $(V_{\text{FS}} - 2 \text{ LSB})$ , the deviation of the difference of the measured values from the value of  $(V_{\text{FS}} - 2 \text{ LSB})$  is the full-scale gain error. The gain error can be

expressed as %FSR or in LSBs. The Gain Error of Figure 10.13 may be determined by the following equation:

$$\text{G.E.} = (V_{\text{FS}} - 2 \text{ LSB}) - (V_{11(\text{meas})} - V_{z(\text{meas})}) \quad (10.12)$$

where  $V_{11(\text{meas})}$  is the last transition voltage,  $V_{z}$  is the first transition voltage, and  $(V_{\text{FS}} - 2 \text{ LSB})$  is the full-scale range of the ADC minus 2 ideal LSBs. For Figure 10.13, the gain error in LSBs is calculated from Equation (10.12) to be:

$$\text{G.E.} = 8 \text{ LSB} - 2 \text{ LSB} - (7\frac{1}{2} \text{ LSB} - \frac{5}{8} \text{ LSB}) = -\frac{7}{8} \text{ LSB} \quad (10.13)$$

at  $V_{11}$ , or  $-1 \text{ LSB}$  at full scale ( $12\frac{1}{2}\%$  of any code).

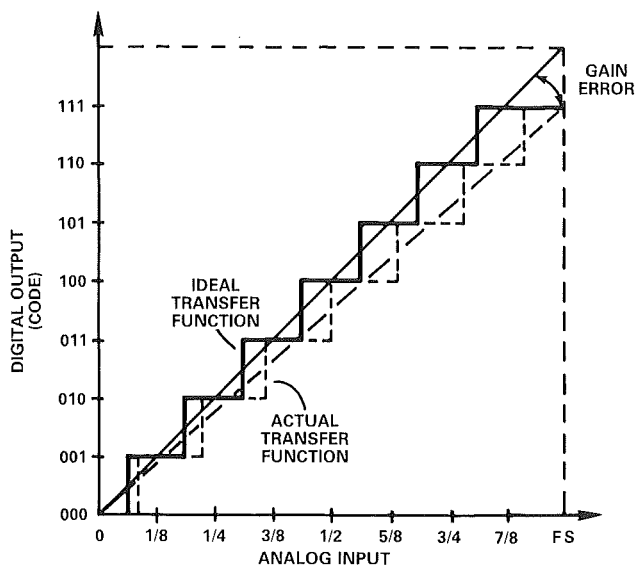


Figure 10.13. 3-bit ADC transfer function with a gain error.

### *Bipolar Offset Error*

The transfer function for an ideal bipolar ADC resembles the unipolar transfer function, except that it is offset by  $-V_{\text{FS}}$  (Figure 10.14). In addition to offset and gain, there is typically one additional parameter specified, bipolar zero.

Bipolar offset error is usually measured as the deviation of the first transition from the ideal, which is usually designed to occur at  $(-V_{\text{FS}} + \frac{1}{2} \text{ LSB})$ ; 1 LSB is equal to  $2 V_{\text{FS}}/2^n$ . As with unipolar offset, the bipolar-offset error is common to all codes, and any nonlinearity or gain error of the LSB must be accounted for in its calculation. The offset error of Figure 10.15 may be determined using Equation (10.10). In the case shown in Figure 10.15,

$$V_{\text{off(Err)}} = -V_{\text{FS}} + 1 \text{ LSB} - 0 \text{ LSB} - (-V_{\text{FS}} + \frac{1}{2} \text{ LSB}) = \frac{1}{2} \text{ LSB} \quad (10.14)$$

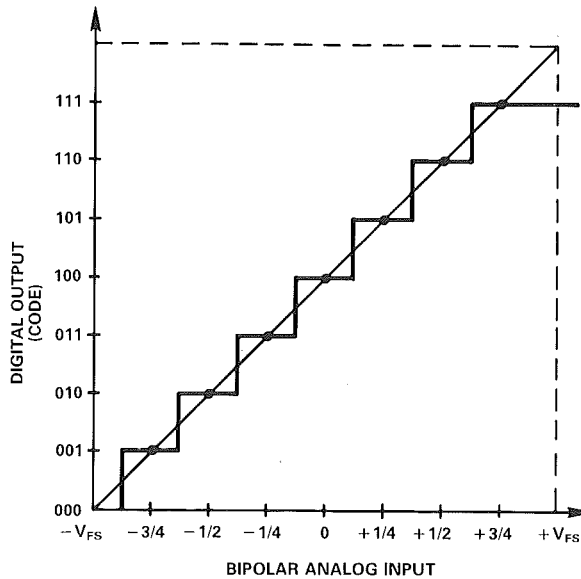


Figure 10.14. Transfer function of an ideal 3-bit bipolar ADC.

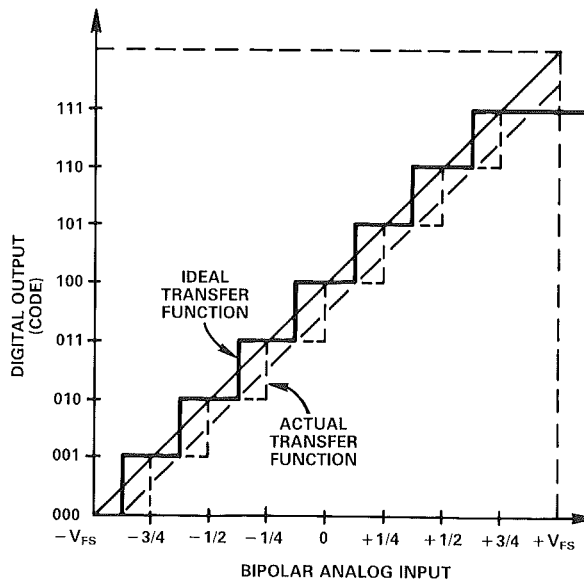


Figure 10.15. 3-bit bipolar ADC with offset error.

### Bipolar Gain Error

Bipolar full-scale error, or gain error, is measured in the same way as unipolar full-scale (gain) error, except that the initial point corresponding to zero for the unipolar case is  $-V_{\text{FS}}$  (Figure 10.16). The gain error of a bipolar-input

ADC is calculated using Equation (10.12). The gain error, in LSB's, of Figure 10.16 is calculated as follows:

$$\text{G.E.} = 8 \text{ LSB} - 2 \text{ LSB} - (7\frac{1}{2} \text{ LSB} - 5\frac{5}{8} \text{ LSB}) = -\frac{7}{8} \text{ LSB} \quad (10.15)$$

at  $V_{11}$ , or 12.5% at any code.

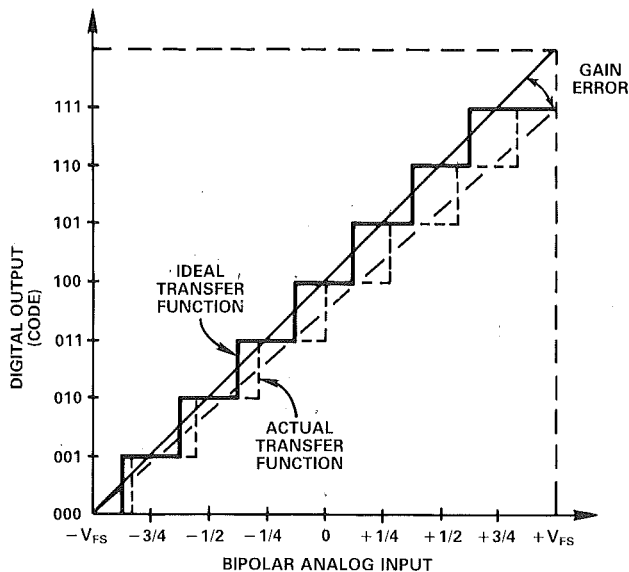


Figure 10.16. 3-bit bipolar ADC with gain error.

### Bipolar Zero Error

The transition that is next most-often measured for bipolar input ADCs is for determining *bipolar zero error*, which is defined as the deviation of the mid-scale transition voltage from the ideal in the vicinity of 0 volts (Figure 10.17). The bipolar zero error may be determined by the following equation:

$$\text{BZE} = V_{\text{zero(meas)}} - V_{\text{zero(ideal)}} \quad (10.16)$$

where  $V_{\text{zero(meas)}}$  is the measured mid-scale (MSB) transition voltage and  $V_{\text{zero(ideal)}}$  is the ideal mid-scale transition voltage. The bipolar zero error of Figure 10.17 is calculated using Equation (10.16) to be:

$$\text{BZE} = -\frac{1}{4} \text{ LSB} - (-\frac{1}{2} \text{ LSB}) = +\frac{1}{4} \text{ LSB} \quad (10.17)$$

Bipolar zero error is not an independent variable; it is the sum of the bipolar offset error, one-half the gain error, and the MSB linearity error. It is usually measured, rather than calculated from the gain and bipolar offset measurements, to avoid errors due to tolerance buildup.



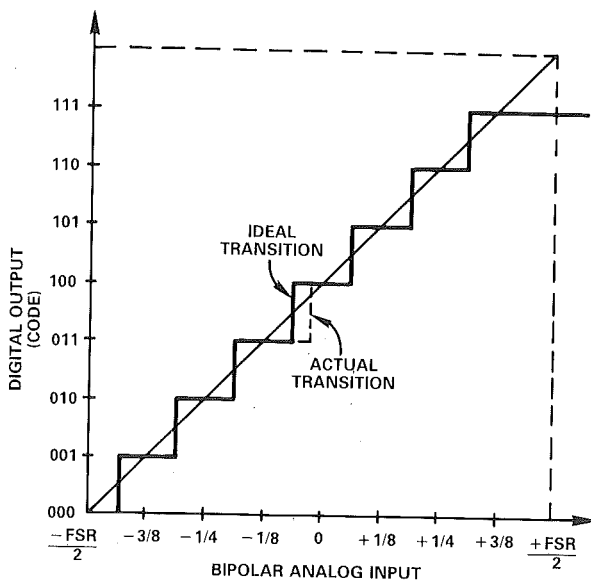


Figure 10.17. 3-bit bipolar ADC with error at analog zero.

### 10.4.3 ADC LINEARITY ERRORS

With most ADC's, the gain and offset specifications are not the most critical ones that determine an ADC's usefulness in specific applications. Typically, offset, gain and zero errors can be calibrated out, in either hardware or software. The most important specifications for the bulk of ADC applications, because they represent irreducible errors, are *differential nonlinearity* (DNL) and *integral nonlinearity* (INL).

#### *Differential Linearity*

Differential nonlinearity in an ADC is defined as the deviation in code width from the value of 1 LSB (i.e.,  $V_{FS}/2^n$ ). If DNL errors are large, the output code widths may represent excessively large and small ranges of input voltages; and if the worst-case DNL is more negative than  $-1$  LSB, the code-width will vanish entirely and the ADC will have at least one missing code. This means that there will be no voltage in the entire full-scale range that can cause that code to appear.

#### *Integral Nonlinearity*

Integral nonlinearity is the deviation of the transfer function from the ideal straight line. Most ADC's are specified with *end-point* INL, i.e., INL specified in terms of deviations from a straight line between the end points of the transfer function (rather than a "best straight line") because it conservatively specifies the worst deviation that will occur for the transfer function; as the description below suggests, it is also easier to measure.

End-point linearity can be measured most easily in terms of the transition points; but it is often defined in terms of the ideal code midpoints. The straight line for *low-side-transition* (LST) linearity is drawn from the offset transition (i.e., from all-0's to the LSB on) to the last transition of the transfer function. The deviation of any transition from its corresponding point on that straight line is the INL of that transition. When *center-of-code* (CC) linearity is specified, the ideal straight line is shifted by  $\frac{1}{2}$  LSB, and the deviation of the center of a code is the INL of that code.

*Best-straight-line* integral nonlinearity is the deviation of any code from a straight line calculated to minimize the worst-case INL errors. The straight line is typically calculated using the least-squares method. This basically involves testing the codes of interest, reducing the data to determine the best straight line, and then retesting to the new straight line.

#### 10.4.4 ADC Test Strategy

##### *Minimum Number of Tests*

Before testing an ADC for DNL and INL, the test engineer must determine which codes must be tested to guarantee performance over the entire transfer function. The problem is similar to that of DACs, in that different ADC architectures will require that different code patterns be tested. In addition, dynamic errors and noise are often significant and unpredictable and require additional tests in the same way bit interactions affect DAC testing.

For example, multi-comparator, or flash, ADCs are constructed using  $2^n$  matched resistors and  $2^n - 1$  comparators. Their architecture requires testing all codes; fortunately (for the test engineer), they are typically low in resolution, seldom having resolutions that exceed 8 bits.

Tracking ADCs are constructed using an internal DAC, a comparator, an up/down counter, and support circuitry. The codes to be tested for DNL and INL are primarily influenced by the DAC design, as dynamic errors are not usually present for moderate clock frequencies. One note of caution to consider when testing tracking ADCs is their susceptibility to noise, as compared to integrating ADCs.

Integrating ADCs are typically high-resolution, high-accuracy devices. They have very good DNL by design. The major sources of INL occur at the inputs of the integrating amplifier and comparator or are due to non-ideal behavior of the integrating capacitor, making it difficult to predict the location of the worst case INL codes. Fortunately, changes in INL will be very gradual, so a simple sampling of codes along the transfer function is usually sufficient to find the worst-case error.

Successive-approximation ADCs have both static and dynamic sources of DNL and INL. These errors come from static nonlinearities of the DAC, long DAC settling time, slow comparators, parasitic capacitance at the summing

junction, and noise. They can require a large number of tests, often repetitively, if noise is significant.

### End-Point Tests

For all ADC's, regardless of architecture, the transfer function's end points must be measured and normalized before linearity testing can begin. Normalization can be done in either hardware or software. Once the appropriate straight line is determined, all that remains is to measure the required transitions or codes and compare them to the ideal.

### Major-Transition Testing

In some rare cases, an all-codes test routine may be required—perhaps even repeatedly, to take into account the effects of noise—to guarantee a tight INL specification in a stringent application. With modern ATE techniques, it is feasible to do this on a sampling basis as part of the production process, after a 100% screen using an abbreviated test routine. Most abbreviated routines are based on the major transitions, plus-and-minus three codes.

The major transitions consist of all the major and minor carries, plus the sums of the most-significant-bits (MSBs). The reason for testing to plus and minus three codes from the major transitions is to check the adjacent codes that may be affected by dynamic conditions of the device under test (DUT).

Figure 10.18 compares the transfer function of an ideal 4-bit ADC with the transfer function of a 4-bit ADC that has DNL and INL errors. The INL in

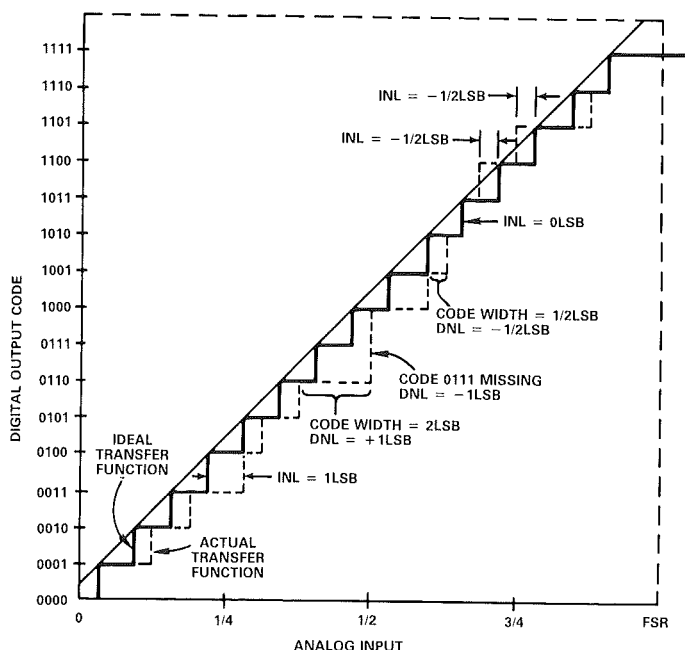


Figure 10.18. 4-bit ADC with linearity errors—both differential and integral (low-side transition).

this case is specified as low-side-transition (LST). The transition to code 0100 is shifted to the right by 1 LSB; this means the LST of code 0100 has integral nonlinearity of  $+1$  LSB.

The transition to code 1101 is shifted left by  $\frac{1}{2}$  LSB; this means the LST of code 1101 has INL of  $-\frac{1}{2}$  LSB. The code-width of code 0110 is 2 LSBs; it means that code 0110 has differential nonlinearity of  $+1$  LSB. The code width of the code 1001 is  $\frac{1}{2}$  LSB; thus, code 1001 has DNL of  $-\frac{1}{2}$  LSB.

Note that code 0111 does not exist for *any* input voltage. This means that code 0111 has  $-1$  LSB DNL and the ADC has at least one missing code.

Figure 10.19 shows the same transfer function, but drawn for a center-of-code (CC) integral-nonlinearity specification. The DNL of all codes remains the same, but notice the change in the values of INL. Code 1101 had  $-\frac{1}{2}$  LSB of low-side-transition INL, but it has 0 LSB of CC INL. Similarly, code 1011's 0 LSB of LST integral nonlinearity becomes  $-\frac{1}{8}$  LSB of center-of-code INL. The same phenomena can be observed for codes 1100, 0100, etc.

Some ADCs are specified with CC and some with LST integral nonlinearity; the choice depends on the ADC design and the intended end use. Users should consult the manufacturer if there is any doubt about which type should be employed for a given device.

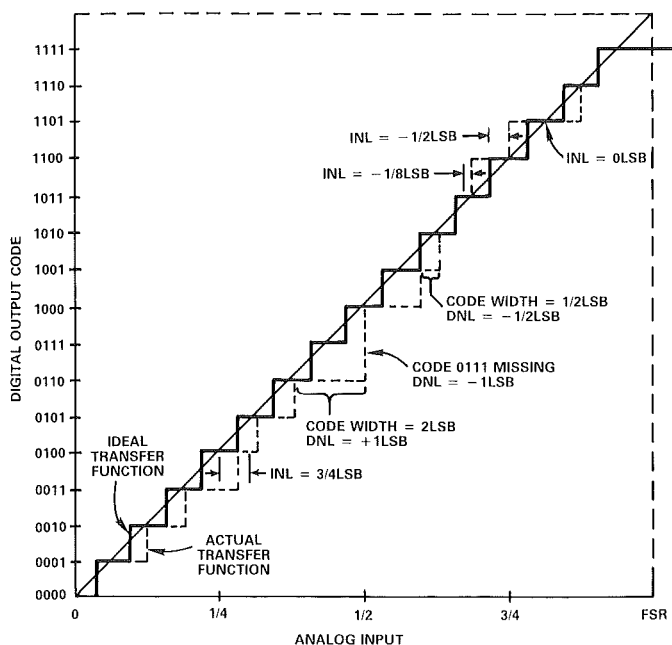


Figure 10.19. 4-bit ADC with linearity errors—both differential and integral (center-of-code).

## 10.4.5 BENCH-TEST HARDWARE

The most common method of determining the DNL and INL on the bench is by using a test circuit that performs a crossplot (Figure 10.20). If a small asynchronous sinusoidal or triangular ac signal—varying at a fast enough rate to provide a persistent image on an oscilloscope, yet slow enough to permit a large number of conversions—is summed with an analog dc voltage and applied to the input of the ADC under test, the ADC's output will be “dithered” about through several codes either side of the code representing the dc voltage. The output of an elementary 2-bit DAC, which decodes the two least-significant bits, is plotted vertically, and the ac analog input is plotted horizontally, producing the repetitive short staircase through codes (. . . 0)00, (. . . 0)01, (. . . 0)10, (. . . 0)11, (. . . 1)00, etc., as shown in the illustration.

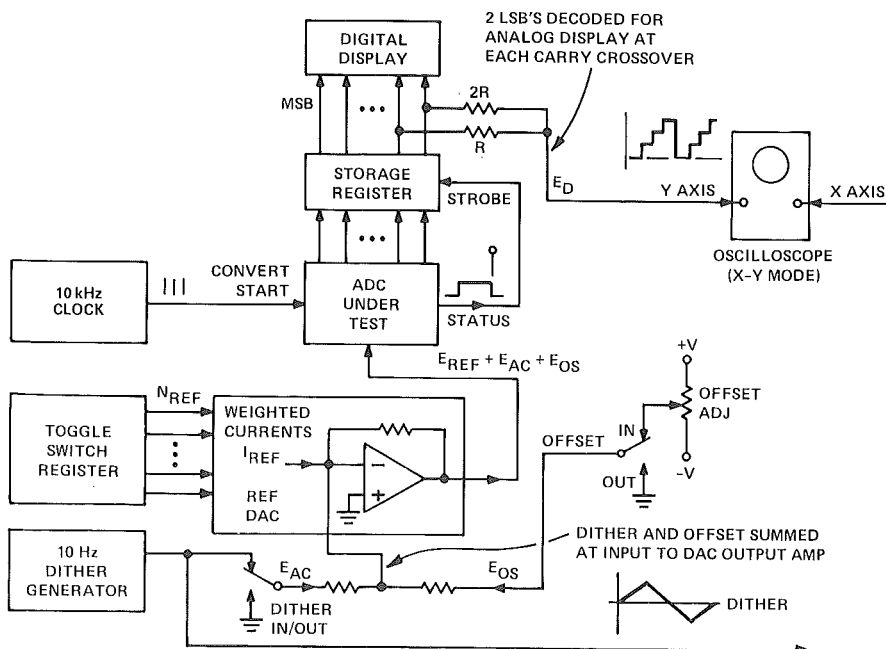


Figure 10.20. ADC crossplot test fixture.

Since the ac voltage serves, over time, to scan through all input voltages within the range of its amplitude, the oscilloscope display is an actual display of the code widths over a short portion of the input voltage range. If the dc voltage is equal to, say, the center of a code, this permits the analog voltages corresponding to the transitions and the center of each code, as well as the adjacent codes, to be readily displayed; this direct display permits determination of device INL and DNL to high accuracy and resolution; it also permits an “eyeball” estimation of noise.

Here's how the dynamic crossplot circuit works: The digital code to be tested,  $N_{\text{ref}}$ , is entered into the reference DAC via the toggle-switch register, thereby applying  $E_{\text{ref}}$ , the analog equivalent of  $N_{\text{ref}}$ , to the analog input of the DUT.

The ac dither,  $E_{ac}$ , and an adjustable dc offset,  $E_{os}$ , are summed with the reference DAC's output. The dither signal has a low frequency in comparison to the conversion rate of the DUT, allowing the digitized output of the DUT to track its analog input to within the  $\pm \frac{1}{2}$  LSB quantization limits, i.e., without introducing dynamic errors. A digital register stores the results of each conversion. The 2-bit DAC is formed, using resistors with weights of  $2R$  and  $R$ , to sum the LSB and the adjacent bit of the stored ADC output. The resulting 4-step analog output, corresponding to the ADC's two least-significant bit states, is applied to the Y axis of the oscilloscope. The ac dither signal is applied to the X axis of the oscilloscope. Figures 10.21b to 10.24f show a number of waveforms obtained using the dynamic crossplot test circuit.

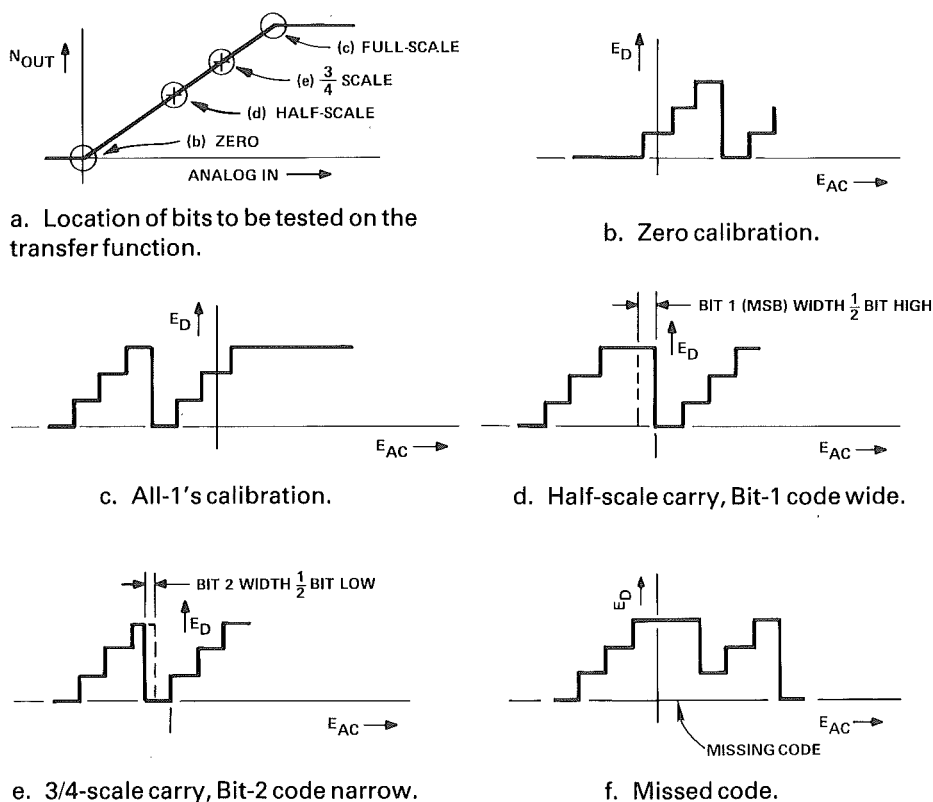


Figure 10.21. ADC crossplot testing.

The device under test is calibrated thus: The CRT beam is first positioned in the center of the screen with the X and Y axis drive signals grounded. Then, with all bits of the reference DAC off except the LSB, adjust the DUT's zero to center the first step of the decoded output staircase waveform, corresponding to the digital code 00 . . . 01 as shown in Figure 10.21b. Next, all bits

except the LSB of the reference DAC are turned on, corresponding to the digital code  $11 \dots 10$ , and the gain of the DUT is adjusted to center the next highest step of the decoded staircase waveform, as shown in Figure 10.25c. Zero and full scale are now calibrated.

Differential nonlinearity and integral nonlinearity at each code transition can be seen and measured visually by examining the width of the codes and the displacement of the transitions, to the left or right, as successive bits are turned on. Transition noise can also be assessed; it appears as a jitter in the location of each code transition.

Some additional points about the crossplot test circuit are worth noting:

- Since only the two least-significant-bits of the DUT's digital output are decoded, the crossplot waveform repeats every four steps. For this reason, the DUT should be originally calibrated to less than 2-bit error before the crossplot is used, so that one can be assured that the desired code transition—and not one four LSBs away—is being displayed.
- The dither waveform shown in Figure 10.20 is triangular—but it could just as well be in a sine-wave, since a linear time relationship is not required in the X-Y display mode for a linear Y vs. X presentation.
- The external storage register shown in Figure 10.20 can be eliminated (at the expense of minor crossplot display degradation) if the conversion rate is reduced so that the time between conversions is large, compared to the conversion period.
- For the configuration of Figure 10.20, typical dither frequencies of 4 to 40 Hz, and conversion clock-frequencies from 10 kHz to 100 kHz have been found useful for crossplot analysis of high speed successive-approximation ADC performance.

### *Static Errors*

Figure 10.21d illustrates the waveform that would appear at the major carry code transition ( $011 \dots 1$  to  $100 \dots 0$ ) of a successive-approximation ADC if the MSB of the internal DAC had  $+1/4$  LSB INL and the summation error of all the lower bits was  $-1/4$  LSB. Notice that the transition representing the code ( $100 \dots 0$ ) is shifted  $1/4$  LSB to the right, and the transition resulting from combinations of the lower bits is shifted  $1/4$  LSB to the left. The result is that the major carry code is too wide by  $1/2$  LSB.

Similarly, in Figure 10.21e, the plot is representative of an ADC where bit two of the internal DAC has  $-1/4$  LSB INL and all the other bits sum to  $+1/4$  LSB INL. The result is a narrow code produced by the transitions on both sides shifting towards one another. Figure 10.21f shows a typical missed-codes signature.

### *Dynamic Errors*

In addition to the errors due to static relationships within the converter, dynamic errors may arise—including missed codes—if the frequency of the clock that times the bit decisions is too high to permit correct decisions to be made. The effects of these errors will also appear in a crossplot. If the ADC's internal timing is controlled by an external clock, dynamic errors may be found by first checking the static errors, then increasing the clock frequency until it affects the crossplot. Experienced converter designers and test engineers can gain considerable information about the internal static and dynamic behavior of the ADC from the nature of the errors revealed by the crossplot.

### 10.4.6 ATE METHODS

Crossplot methods of testing ADCs work well for engineering analysis or low-volume production testing, but they are slow and tend to be specialized to particular device types. There are many differences among ADCs, and the job of testing devices in outgoing or incoming inspection could become a complicated—if not hopeless—task, even on a sampling basis, without automatic test equipment (ATE). A truly universal ADC test setup should be able to test any of the various types of converter with minimal hardware changes. Here are some of the many differences:

- *Input ranges:* 0 to 10V,  $-5$  to  $+5$ V,  $-10$  to  $+10$ V, and  $-2$  to  $+2$ V are typical. A single ADC may be capable of a combination of input ranges.
- *Output codes* may be binary, offset binary, ones complement, twos complement, sign-magnitude, seven-segment decoded format, or a complement of any of these. What's more, an ADC can have more than one output format (for example, binary is converted into two's complement simply by inverting the MSB).
- *Output modes:* An ADC's output also may be read in different modes. A device may have a serial (non-return-to-zero) data output or a (12-bit) byte/nibble format for 8-bit-microprocessor-compatible output; and it may be necessary to check all digital input and output lines for meeting loading and timing specifications.

A variety of ATE techniques have evolved; the best method to use generally depends on the ultimate end-use of the ADC and the practical considerations of implementing the technique. For example, statistical techniques have the advantage of not requiring accurate analog measurements. Digital signal processing techniques, or the analysis of reconstructed waveforms, may be relevant to the end-use in radar, video, or audio applications.

The technique in most widespread use, evolved to handle converters for the large medium-speed data acquisition, instrumentation, and control markets, is a digital feedback approach, in which the input of the ADC is driven to



selected output code transition voltages in a fashion similar to the crossplot scheme.

### Digital Feedback Loop

A block diagram of a simple digital feedback loop that can be used on a tester with relatively slow digital I/O and high-accuracy analog measurement capability is shown in Figure 10.22. It consists of the converter under test, a decision maker, which compares the ADC's digital output with the programmed digital setpoint, and an integrator with switched polarity and controllable gain.

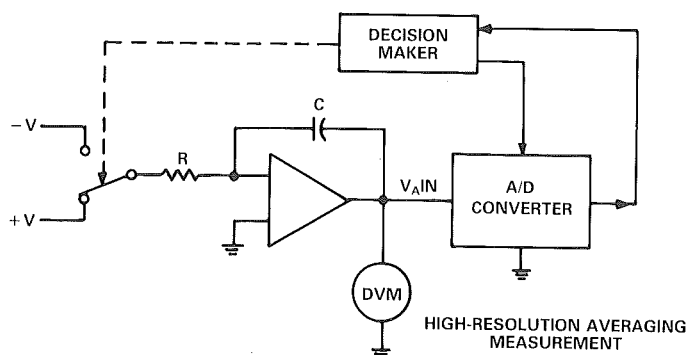


Figure 10.22. Feedback loop to measure transition voltage.

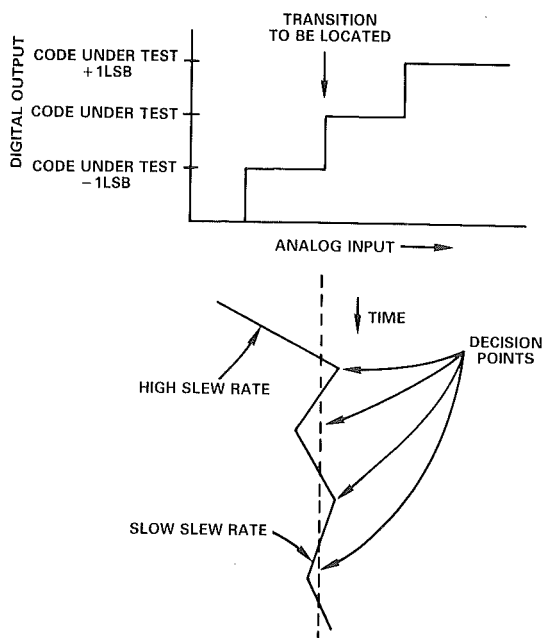


Figure 10.23. The integrator homes in on an average analog output voltage that corresponds to the desired code.

The analog input is made to lock onto a transition voltage by controlling the polarity of a ramping integrator output (Figure 10.23). In a typical sequence, suppose the digital code is below the transition being tested. The decision maker switches the integrator to the negative input, causing the integrator output to increase in the positive direction. On each successive conversion, a new decision is made; when the code is too high, the integrator is switched to ramp in the reverse direction; the integrator speed is also reduced, in order to increase the sensitivity of the measurement.

The decision-maker could be a simple digital comparator. It controls the ramp rates and polarities so the analog input voltage eventually dithers around the transition being sought. A high-resolution dc voltmeter reads the average value of the integrator output to determine the mean transition voltage.

Besides simplicity, this approach offers the advantage that the input voltage has infinite resolution because it is analog. Also, it integrates out any noise in the transition by naturally seeking the 50% point, if the positive and negative ramp rates are tightly matched. But there are drawbacks: besides requiring equal ramp rates, the analog measurement must have high resolution and accuracy (16 bits); and the low-level triangular wave must be averaged in the measurement of the DUT input level. Such measurements are not fast enough for many uses, even with modern measurement systems.

A further improvement to this technique combines the infinite resolution of analog dithering with the high accuracy of a 16-bit reference DAC, allowing the integrator to be used for a low-resolution difference measurement, instead of controlling system accuracy (Figure 10.24). The reference DAC sets the desired transition voltage, and the integrator homes in on the difference be-

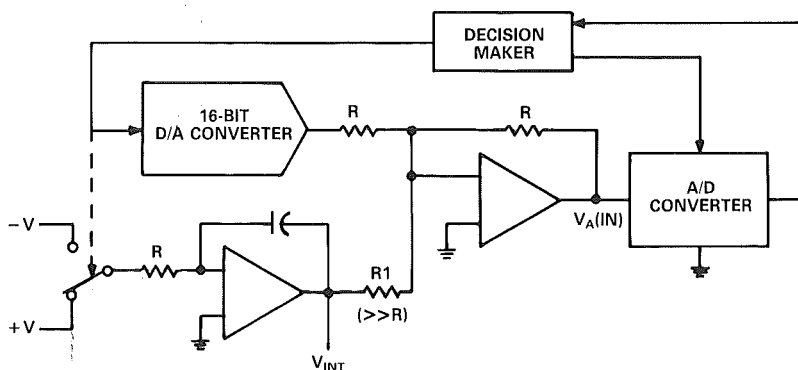


Figure 10.24. Error loop with a 16-bit reference DAC to provide an analog set point to correspond to the digital set point. The integrator reads out the ADC's transition error.

tween the desired and actual transition voltages. The difference is measured by a digital voltmeter (requiring less resolution than that in 10.22). The constraints on—and limitations of—the integrator still apply, however, and limit the tester's speed and flexibility.

These limitations disappear if the integrator is replaced by a 12-bit “dither” DAC, to form a digital tracking loop (Figure 10.25). This approach offers many advantages; the most important is that the dither DAC provides resolution comparable to using an analog integrator but with much greater speed and flexibility. In addition, the analog input presented to the DUT is completely defined digitally; no analog measurement is needed.

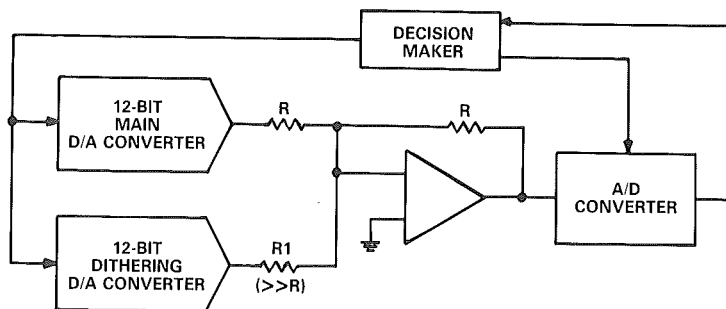


Figure 10.25. Set-point DAC and dither DAC combine in digital control loop to find ADC transition error.

The output of the 12-bit dither DAC sums with the main DAC's output to produce the ADC's input voltage. If  $R_1 = 100 R$  (as in this example), the LSB of the dither converter has an effective resolution of 0.01 LSB (of 12 bits), which is more than adequate for 12-bit testing. Actually,  $R_1$  may be further reduced to optimize the resolution for different applications. At maximum attenuation ( $R_1 = 500 R$ ), the effective resolution of the dithering DAC becomes 10 microvolts. Since  $10 \mu V$  corresponds to 0.06 LSB on a 16-bit 10-volt-span ADC, converters having greater than 12-bit resolution can be tested for all parameters, with INL limited only by the accuracy of the main DAC.

When this scheme is used in a computer-based automatic test system, the decision maker can be more “intelligent” than just a digital comparator, and the function could, in principle, be taken over by the test-system CPU. However, the CPU is generally programmed in some high level language, such as BASIC, which would slow down the execution of linearity routines or the search for all 4,095 code transitions of a 12-bit ADC. Instead, if the processing is distributed—with a slave microprocessor as the decision maker—many further advantages in speed and flexibility will accrue. For example, the slave processor, programmed in machine language, would determine all transition locations, while the CPU need only tell the slave how many approximations to use to create an average digital value for the transition of the “code under test” (CUT).

Figure 10.26 is the functional block diagram of a family test board dedicated to ADC testing for use in the Analog Devices LTS-2000-series of general-purpose benchtop component testers. Its operation is controlled by a slave processor, which receives instructions downloaded from the mainframe's central-processing unit.

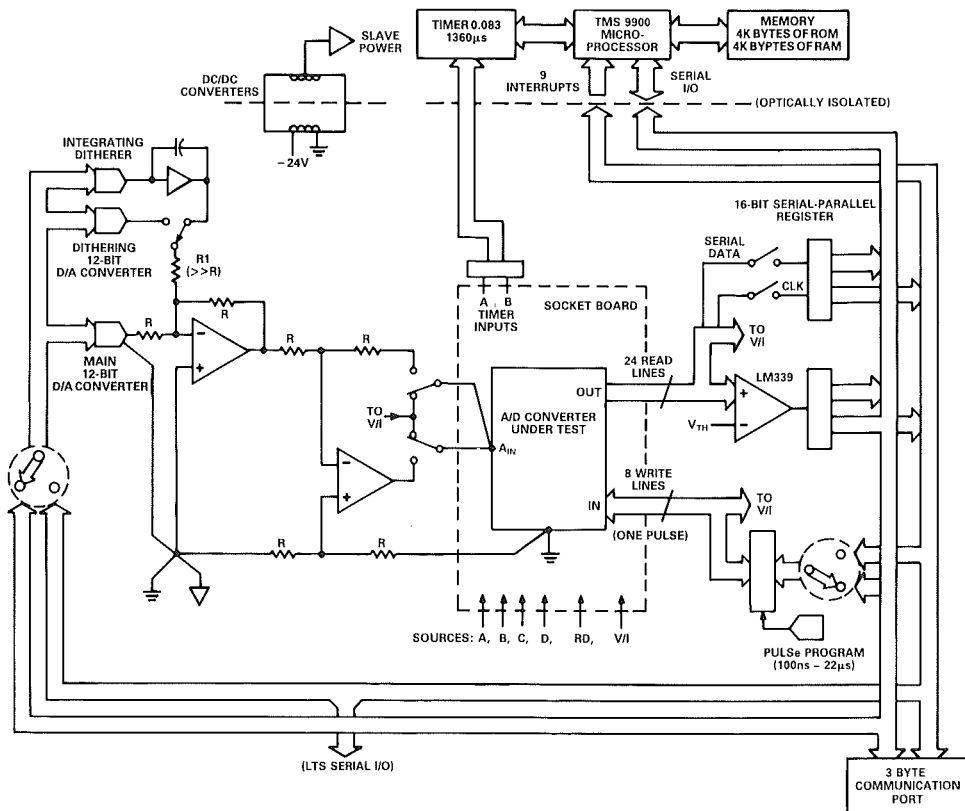


Figure 10.26. A/D Converter family test board for an LTS-2000-series benchtop automatic test system.

The slave processor, therefore, offers the advantage of raw processing speed. Because it is dedicated to testing, test time is independent of the system overhead and hardware settling time. A distributed-processing system also maximizes flexibility for testing the linearity of ADC's. For example, the slave processor may be told to report to the CPU values for all codes tested, or only for codes that fail, or only for the two codes having the greatest positive and negative linearity errors. Bit values in the variable responsible for code reporting can control whether linearity is to be tested at the transitions or at the center of the codes.

With the slave processor, a 12-bit, 5- $\mu$ s ADC can be tested for linearity of all codes (reporting only worst-case codes) in less than 15 seconds to a sigma (rms deviation) repeatability of 0.04 LSB.

The slave processor also has the ability to map a transition. A digital value may be entered and the slave engaged to perform a great many conversions and report the percentage of conversions into the code under test for voltages in the vicinity of the transition. (See Figures 10.27 and 10.28) The input may be stepped incrementally by the programmer and the resulting values plotted on a CRT to present the transition graphically as a function of voltage and

percentage conversion into the code being tested for voltages in the vicinity of the transition.

The circuit also contains an integrating dither that may be used to create a crossplot of the DUT (much like the crossplot circuit of Figure 10.20). The slave uses the integrator to sweep across a selected number of codes around a selected code. The two LSB's of the DUT are decoded to create four levels at the DAC dither. The outputs of the DAC dither and the integrating dither are connected to an oscilloscope's Y and X inputs, respectively, to produce the crossplot.

*No-missing-codes* is the most important requirement for most ADC applications. Until recently, the manufacturer's ability to guarantee the presence of all codes by actual 100% test has been hampered by the test time required to find all codes. A statistical technique sometimes used is called a ramp-input, fill-the-buckets method.<sup>4</sup> In this scheme, a free-running, large-signal, low-frequency waveform is fed into the DUT. The CPU keeps track of the number of times each binary code appears in the output. This technique, while faster than the crossplot or analog integrator methods, cannot operate at the speed of the distributed-processor ADC test circuit.

By virtue of the slave processor and the dither DAC, the existence of all codes of the DUT can be determined very quickly: on the order of 2 seconds for a 12-bit ADC. This routine works by a controlled search for the codes. It starts by making an intelligent guess as to the location of the code. If the code is not found, the processor either increments or decrements the dither DAC by counting or by a successive-approximation routine, depending on the output code just found. It will seek a code down to a resolution of 0.03 LSB before the code is considered missing. Once a code is found, the main DAC's output is increased by one LSB of the device under test, and the process is repeated for the new code.

## 10.5 PRACTICAL CONSIDERATIONS

Now that the basics of ADC testing have been discussed, it's time to consider some of the practical problems encountered when trying to test an ADC. These problems usually fall into one of four categories: nonlinearities in signal-conditioning circuits, grounding and decoupling errors, inattention to dynamics, and incorrect definition of parameters.

### 10.5.1 TRANSITION UNCERTAINTY

In the preceding text, except for an occasional mention of noise, a transition has been treated as if it were sharp, occurring at a unique voltage. In fact, transitions appear wide or blurry on a crossplot display, due to noise and/or finite internal comparator gain.

<sup>4</sup>D. Philip Burton, "Checking A/D Converter Linearity," *Analog Dialogue* 13-2 (1979): 10.

The effects of noise (occurring in either the signal or the converter, or picked up in the wiring) are to introduce an uncertainty in the precise determination of the analog input values at which the output code transitions take place, and to, in effect, increase or reduce the quantization band. The nature of the effects of quantization and noise uncertainty errors is shown in Figure 10.27.

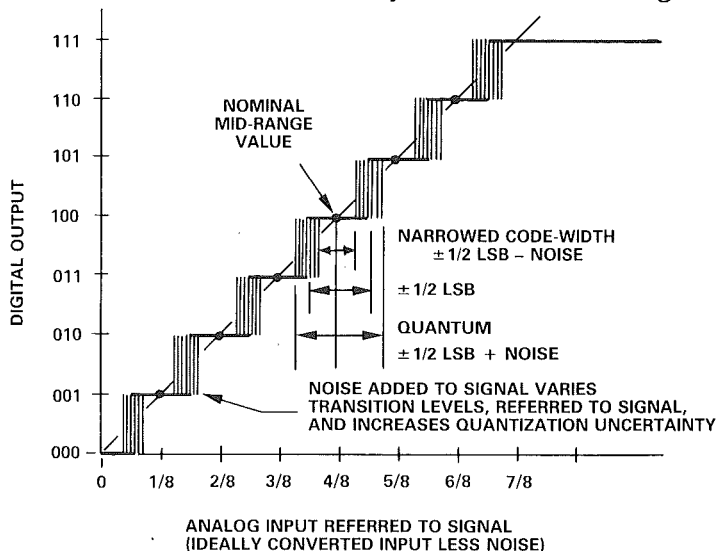


Figure 10.27. Quantization and noise uncertainty error.

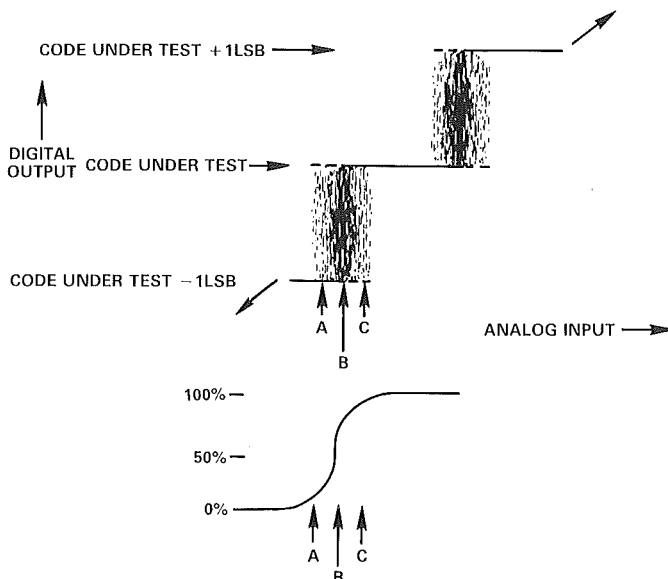


Figure 10.28. Statistical definition of code transition.

The model of a transition can realistically be drawn as a probability function (Figure 10.28). Starting (say) near code center, all (or nearly all) conversions are to the nominal code. Then, as the input voltage is slowly increased toward

and through a transition, the ADC converts more and more frequently into the next code. The most-common definition for the location of the transition is that input voltage which results in 50% probability of conversion into each of the two adjacent codes.

Taking this into account, servo-loop and test hardware—and software—must be designed to insure repeatable readings consistent with the definition. For example, if the ramp size of Figure 10.23 is small enough—and given enough time—the analog integrator output will settle to the voltage at which the average current in the integrating capacitor is zero. This will be the 50% transition voltage if the input current sources are exactly equal.

In digital dither loops, more flexibility is available in choosing the search algorithm. It has been found more efficient to mathematically average the results of multiple successive approximations, rather than imitate the analog integrator by simulating a linear triangle wave.

### 10.5.2 HARDWARE CONSTRAINTS

It is inherently harder to design and build a successful test circuit for an ADC than for a DAC because of the dynamic nature of the ADC. In testing a DAC, the analog measurement can be delayed until the DAC and all the analog support circuitry have settled to their final states. An ADC, on the other hand, converts at its own speed without regard for the condition of the signal or the support circuitry. This makes the need for proper grounding and power-supply decoupling critical and places severe demands on the analog input buffer.

#### *Grounding*

It is good practice to establish one point as the analog reference point. All analog supply decoupling should connect to this single point via separate PC board foils or wires. When testing ADC's, every attempt should be made to arrange circuit topology in such a way that the analog ground reference point and the analog ground connection of the ADC are located as close to the ADC as possible (Figure 10.29).

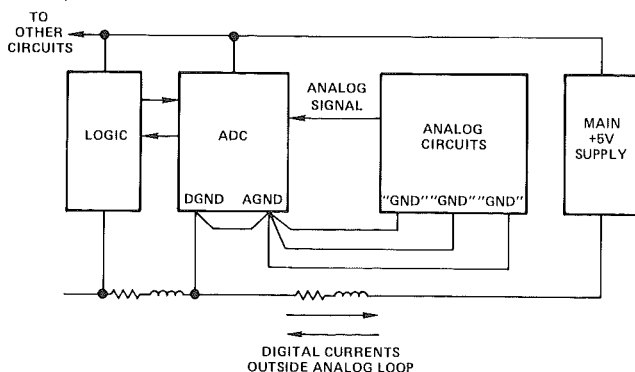


Figure 10.29. Proper grounding arrangement.

### Input Buffer

The most common problem encountered is the inability of the buffer amplifier to reproduce the outputs of the reference DAC and the dither circuit at the input of the ADC. The amplifier must have the rare combination of excellent dc precision and fast dynamic settling.

The input impedance of many ADCs is low and—worse yet—changes abruptly during the conversion process. For example, in successive-approximation converters, the input current is compared to the internal DAC's output current. The comparison point (summing junction of the comparator) is diode-clamped, but it may swing plus and minus several hundred millivolts. This gives rise to a modulation of the input current (Figure 10.30).

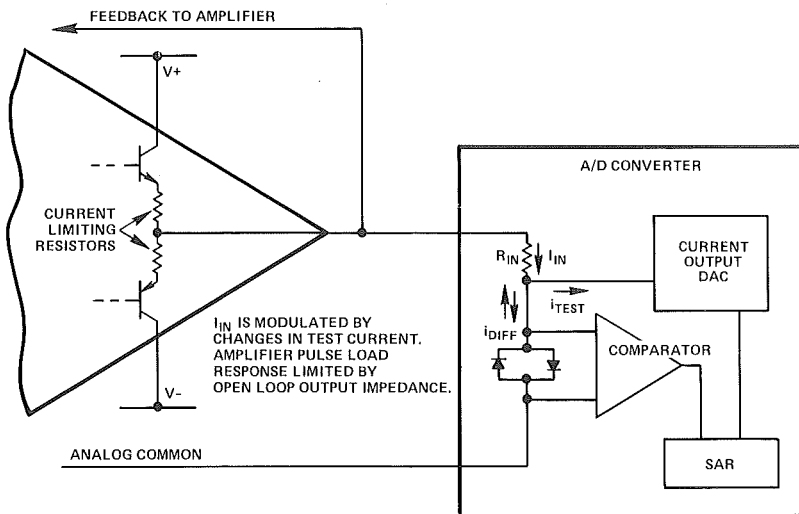


Figure 10.30. The problem of driving a successive-approximation ADC; transient load currents produce changes in output voltage.

For example, an amplifier supplying 2.5 volts to an ADC in the 10-V unipolar range will experience a 32% increase in load current when the ADC tries Bit 2. The amplifier will have to re-establish 2.5-V output—to well within the LSB—before the internal comparator is strobed, or an error in the output code will result. This requires an output impedance of under 10 ohms at all frequencies up to 2 MHz for a modest-speed (12- $\mu$ s) 12-bit ADC with a 5k $\Omega$  input resistor.

It is well known (and expected) that the output impedance of a feedback amplifier is reduced by its loop gain. However, at high frequencies, where the loop gain is low and phase shift affects feedback polarity, the amplifier output impedance rises from its dc value to approach or exceed its open-loop value. In the case of most IC amplifiers, the open loop output impedance is typically 100 to 200 ohms because of the current-limiting resistors. Even a few hundred



microamperes, reflected from the change in the load presented by the converter, can introduce errors in the instantaneous input voltage. If the bandwidth of the amplifier is sufficient to handle the ADC's conversion speed, the output will return to the nominal voltage before the converter makes its comparison, so that little or no error is introduced.

However, many precision amplifiers have relatively narrow bandwidth. This means that they recover very slowly from output transients. Naturally, precision amplifiers are more likely to be used in testing high-resolution ADCs, where small dc errors are less tolerable. As a result, fast, high-resolution test systems may suffer from amplifier output-transient errors. A wideband IC amplifier, such as the AD509, which does not include output current-limit resistors, is often sufficient, as is the more accurate, slightly slower AD OP-27. A hybrid or discrete unity-gain buffer amplifier may be added inside the amplifier loop (Figure 10.31) to improve the load transient response. High-linearity sample-and-hold amplifiers, such as the AD585, also are designed to have low output impedance and fast loop response.

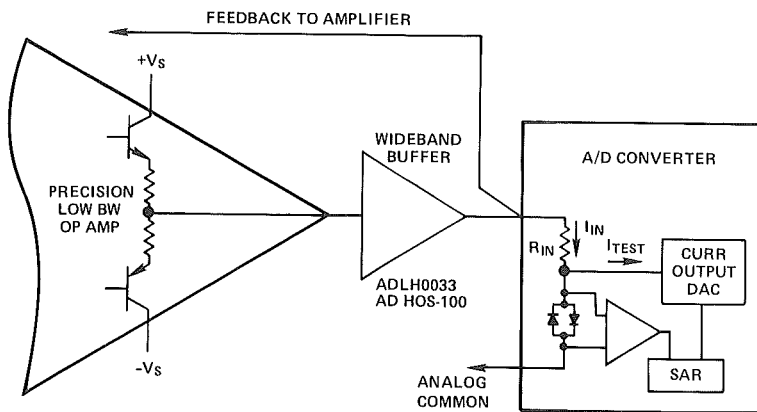


Figure 10.31. Wideband buffer inside-the-loop will drive the ADC.

Another dynamic problem often arises when testing ADCs that have multiple input ranges. Depending on the architecture of the inputs of the ADC, there are different ways of connecting unused input pins. Some ADCs require the unused pins to be grounded. This is typically to eliminate noise from being introduced into the summing junction through the unused input resistors. Other ADCs require that the unused input pins be left unconnected. This is typical because the input resistor is still part of the actual analog input. Any parasitic loading on this pin can result in unpredictable device performance. In *either* case, inattention to these details can result in inaccurate conversions or even missing codes, rendering testing basically useless.

### 10.5.3 TESTING UNDER DYNAMIC CONDITIONS

The bench version of the crossplot tester, and its ATE counterpart—the digital feedback circuit—test the ADC with essentially a dc signal at its input.

However, static testing is not sufficient for devices intended to be pushed to their limits at high speed, such as video ADC's; converters can demonstrate virtually ideal digitizing transfer functions under dc or low-frequency ac stimulation, but under dynamic stress, i.e., ac test signals approaching the Nyquist sampling-rate limit,  $f_s/2$ , they often exhibit otherwise hidden shortcomings, such as missing codes, non-monotonic conditions or linearity errors.<sup>5</sup>

Therefore, some form of dynamic testing is required, albeit it employs standards and procedures differing from those of industry-accepted static testing for lower speeds. Users tend to focus only on those ac specifications that highlight performance in a particular video-converter application. For example, *differential gain and phase* are paramount in digital-video uses, and *signal-to-noise ratio* dominates evaluation of devices aimed at data-communication tasks. More on this subject will be found in Chapter 13.

### Analog Waveform Reconstruction

Traditionally, dynamic testing took the form of a waveform reconstruction technique, which connects a high-performance d/a converter to the video a/d converter under test and permits dynamic performance measurements with conventional analog test equipment. To obtain valid test results, however, the DAC's static and dynamic performance must exceed that of the a/d converter by two bits or more.

Fortunately, because many DACs achieve such higher performance, back-to-back a/d-to-d/a testing proves successful (Figure 10.32). A deglitcher connected to the DAC's output removes unwanted harmonics caused by DAC glitches or analog-output discontinuities. Essentially a track/hold amplifier, the deglitcher switches to its *hold* mode immediately before the DAC gets updated.

Probably the most powerful indicator of an A/D converter's dynamic performance is its signal-to-noise ratio (SNR). When stimulated by a spectrally

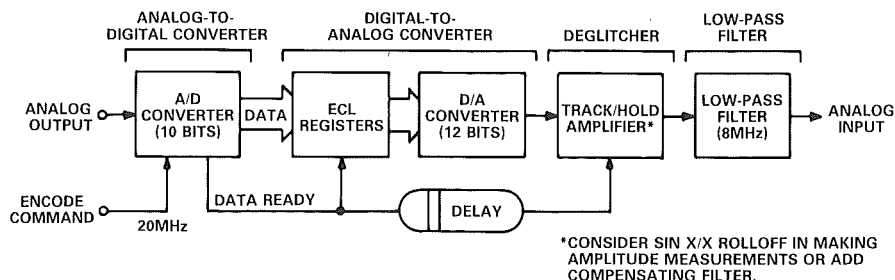


Figure 10.32. Testing an a/d converter by the use of a higher-performance back-to-back DAC.

<sup>5</sup>Walter Kester, "Test Video A/D Converters Under Dynamic Conditions," EDN, August 18, 1982.

pure sine wave, an ideal a/d converter generates  $q/\sqrt{12}$  rms quantizing noise in an  $f_s/2$  bandwidth, where  $q$  equals the weight of the least-significant bit (LSB). This rms noise level is independent of the input sine wave's level and frequency as long as the level lies within the a/d converter's operating range.

Theoretically, the logarithmic expression of the ratio of a full-scale sine wave's rms level to an ideal  $N$ -bit a/d converter's rms quantizing noise (measured over an  $f_s/2$  bandwidth) equals

$$\text{SNR} = 6.02 N + 1.8 \text{ dB} \quad (10.19)$$

Practically, though, an a/d converter's noise floor increases with the full-scale sine wave's increasing input frequency; the corresponding SNR thus decreases. Conversely, holding the input frequency constant but reducing the sine-wave amplitude decreases the a/d converter's noise floor.

A/D-converter SNR test results can be displayed and analyzed in several ways. One way is to plot SNR versus sine-wave frequency for a constant-amplitude full-scale sine-wave input. SNR can also be plotted versus input-signal amplitude for a fixed sine-wave frequency. The two plots can be combined (Figure 10.33) to form a set of curves that permit the number of effective bits of resolution for various amplitudes and frequencies to be determined and compared with the theoretical values.

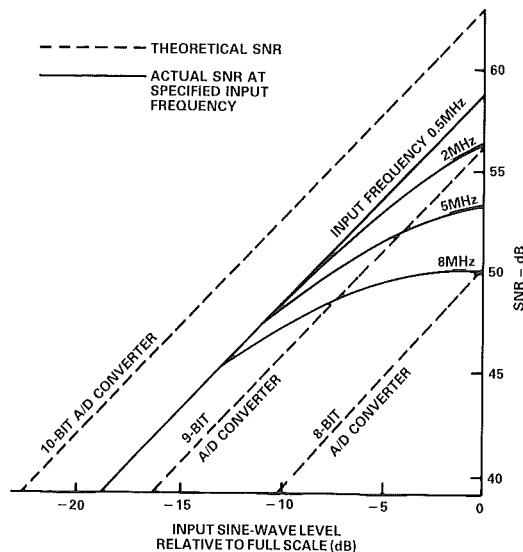


Figure 10.33. Signal-to-noise ratio vs. sine-wave level and resolution of an ADC. These plotted curves help analyze a video a/d converter's theoretical and actual SNR test results.

Note that the SNR can be measured for input signals greater than the Nyquist limit,  $f_s/2$ . However, it is important to be aware that the fundamental sine wave then appears as an alias component within the  $f_s/2$  bandwidth. For example, a 12-MHz sine wave's in-band component when sampled at 20 MHz occurs at 8 MHz.

*Digital Waveform Analysis*

In modern ATE, digital processing is cheaper to provide than a precision dynamic AC measurement capability. In these systems, the digital output stream of the ADC under test is sent directly to a high speed buffer memory for later analysis by a computer or array processor. The computer may simply create a histogram of the output codes, which can be analyzed for gain, offset, missing codes and linearity errors. DSP techniques, such as the fast Fourier transform, may be employed to do spectral analysis of the digital output table to determine signal-to-noise ratio, differential phase and differential gain, in addition to the above characteristics.

# Chapter Eleven

## Specifying Converters

The applications for digital data-handling equipment and the products of the conversion-and data-acquisition industry have spawned a multiplicity and diversity of companies, product lines, and products. We find it sobering,\* though not a little gratifying, to discover that (as a major manufacturer, with a reasonably complete line of monolithic, hybrid, and modular products) we can deliver hundreds of distinct converter types—of which a large number are in the “recommended-for-new-designs” category, and that the line is growing substantially each year.

Thus, the very large number of converter products available in the marketplace, even from a single manufacturer, can overwhelm even the most informed engineer, when faced with the problem of selecting a device, or a group of devices, for a given application.

Interpretation of the specifications adds another dimension to the task, which is further complicated by the difficulty of finding standardized definitions of specifications that all manufacturers can agree upon.

To remedy this situation, and attempt to make the system designer’s job of finding the “right” converter a little easier,† this chapter lists some of the elements of the decision—and steps a user can take to help “home in” on a near-optimum selection. In this chapter are also summarized interpretations of the

\*It’s even more disconcerting to realize that this paragraph appeared in the first edition of this book in 1972, when the Analog Devices product line was much smaller, with the words, “. . . we can deliver some 250 distinct D/A[!]  
converter types, . . . growing by 75 types per year.”

†It’s possible that some of the points raised here, if previously unanticipated by the reader, may actually make the initial selection more involved, with the benefit that problems will be fewer at a later (and more expensive) stage.

specifications, consistent (it is to be hoped), not only with the previous three chapters and with engineering practice at Analog Devices, but also with interpretations that may become accepted as standard within the industry.

For the convenience of the engineer who may seek orientation to some of the categories of devices available off-the-shelf, Tables 1 and 2 are abbreviated selection charts containing a sampling of popular general-purpose integrated-circuit converter-product families manufactured by Analog Devices, Inc., in 1984. They are based on the a/d and d/a converter sections of the 1984 Analog Devices *Databook*, which contains comprehensive selection guides, complete specifications, descriptions, and applications information for converters and a wide variety of converter-related products. The latest edition available should be consulted when specific designs are being considered. The reader is invited to request a copy from the manufacturer's home or local sales offices. The conscientious engineer will also seek comparable data from other manufacturers.

Finally, a brief example of a data-acquisition design process is given, based on the suggestions in this chapter.

## 11.1 TWO BASIC FACTORS

The two key factors in choosing the right device are:

*Completely define the design objectives.* Consider all known objectives and try to anticipate the unknowns that will pop up later. Include such factors as signal and noise levels, required accuracy, throughput rate, characteristics of the signal and control interfaces, environmental conditions and space factors, and anticipate budgetary limitations that may force performance compromises or a different system approach.

*Understand what the specs mean.* It is essential to have a firm understanding of what the manufacturer means by his set of specifications. It should not be assumed (in 1985) that any two manufacturers mean the same thing when they publish identical numbers defining a given parameter. In most cases, the manufacturer has honestly attempted to provide accurate information about his product. This information must be interpreted, however, in terms meaningful to the user's requirements, which requires a knowledge of how the terms are defined. Two examples that give an insight into how differences arise are included and discussed at length in the Specifications section: *linearity* and *temperature coefficient*.

## 11.2 DEFINING THE OBJECTIVES—APPLICATION CHECKLISTS

### *General Considerations*

- A. Accurate description of input and output
  - 1. Analog signal range; source or load impedance

2. Digital code needed: Binary, twos complement, BCD, etc.
3. Logic-level compatibility: TTL, CMOS, etc., logic polarity (unless otherwise noted, logic levels mentioned in Analog Devices publications are standard TTL, positive-true)
- B. Data throughput rate
- C. Control and data-interface details or constraints
- D. What does the system error budget allow for each block?
- E. What are the environmental conditions: temperature range, supply voltage, re-calibration interval, etc., over which the converter should operate to the desired accuracy?
- F. Are there any special environmental conditions that must be coped with? EMC, high humidity, shock and vibration, and cramped space are a few.
- G. What are the bounds of integration for the purchased portion of the system? Turnkey system, real-time interface, data-acquisition subsystem, subassemblies, components? What are the hardware/software, analog/digital tradeoffs?

In addition to the above general considerations, there are specific items to consider when choosing each block in a system.

#### *Considerations for D/A Converters*

- A. What resolution is needed? How many bits (e.g., 8, 10, 12, etc.) of the incoming data word must be converted? To what degree of accuracy, linearity, etc.?
- B. What logic levels and codes can be provided to the DAC? (The most popular logic system is TTL, and the most-frequently used codes are binary, twos complement, offset binary (twos complement with a complemented MSB), as outputs of systems, and BCD, usually derived from digital voltmeters or thumbwheel switches.) Is digital input serial or parallel?
- C. What kind of output signal is needed: a current or a voltage? What is the desired full-scale range? (Most DACs are available with either current output—at very high speed—or voltage output, with the added delay of an internal operational amplifier. Voltage-output DAC's are the more convenient to use but—unless designed specifically for high speed—will serve only in applications not calling for submicrosecond settling times. Current-output DAC's are used in applications where high speed is more essential than stiff voltage output, such as circuits with comparators (e.g., A/D converters), or where fast amplification is to be provided externally (e.g., via CRT deflection amplifiers).
- D. What kind of reference is needed, fixed (internal or external) or variable (multiplying DAC)? For multiplying DACs, how many quadrants are needed, and how arranged (1-quadrant, 4-quadrant, 2-quadrant digital, 2-quadrant analog)?

- E. What is the nature of the digital interface? What are the speed, requirements? What is likely to be the shortest time between data changes? After a change in the digital input data, how long can the system wait for the output signal of the DAC to settle to the desired accuracy for a full-scale change? For a 1-bit change at the major carry? Are switching transients of any consequence? Can they be filtered? Must they be suppressed (i.e., deglitched) within the DAC? What is the analog signal feedthrough requirement for multiplying DAC's at low frequencies? At high frequency?
- F. Over how wide a temperature range (at the device, including its internal temperature rise) must the converter operate? Over how much of this range must the converter perform essentially within its specifications with readjustment? What degradation of specifications is permitted (gain vs. linearity, etc.)?
- G. How stable are the terminal voltages of the power supplies that will power the DAC? How stable should they be? Is the power-supply sensitivity specification adequate to hold errors from this source within reasonable limits? Are there constraints on converter dissipation?

Though no list can be complete, the above items will be the minimum consideration in any more-complete tabulation.

#### *Considerations for A/D Converters*

The process of selecting an a/d converter is similar to that involved in the selection of d/a converters. Some of the following considerations are analogous to those for DACs, and others are unique to ADCs.

- A. What is the analog input range, and to what resolution must the signal be measured.
- B. What is the requirement for linearity error, relative accuracy, stability of calibration, etc.?
- C. To what extent must the various sources of error be minimized as ambient temperature changes? Are missed codes tolerable under any conditions?
- D. How much time is allowed for each complete conversion?
- E. Is the reference to be fixed, adjustable, or variable (ratiometric measurement)?
- F. How stable is the system power supply? How much error due to power-supply variation is tolerable in the conversion system? Are there constraints on converter dissipation?
- G. What is the character of the input signal? Is it noisy, sampled, filtered, rapidly varying, slowly varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? What conversion circuit philosophies are acceptable for—or indicated by—the application? (e.g., successive-approximation, dual-slope inte-



gration, counter-&-comparator, etc. As a rule, integrating types are best for converting noisy input signals at relatively slow rates, while successive-approximation is best suited to converting sampled or filtered inputs at rates up to 1MHz. Counter-comparator types provide lowest cost but may be both slow and noise-susceptible; they are useful for peak followers and sample-holds that employ digital storage.)

- H. What is the bus width and format of the digital interface? Parallel, byte-serial, serial? Buffered, three-state? What kind of logic? ECL, CMOS, TTL?

### *Considerations for Analog Multiplexers and Sample-Holds*

When a sampled-data-system is to be assembled, in which one a/d converter is time-shared among many input channels by the use of a multiplexer and sample-hold, their contribution to system performance errors must be taken into account. These accessory devices are discussed elsewhere, but they are also discussed briefly in this chapter because of their relevance to the converter selection process.

#### *Multiplexers*

- A. How many input channels are needed? Single-ended or differential? High-level or low-level? What dynamic range?
- B. What kind of hierarchy is used, if a great many channels are involved? What is the addressing scheme?
- C. How much time is needed for settling to desired accuracy when switching from one channel to another? Maximum switching rate?
- D. How much ac crosstalk error between channels is allowable? At what frequencies?
- E. What error is produced by the leakage current flowing through the source resistance?
- F. What will be the multiplexer “transfer” error, produced by the voltage divider formed by the *on* resistance of the multiplexer and the input resistance of the sample-hold. Is the multiplexer active or passive (i.e., does it have an output amplifier, or is it simply a set of switches?)
- G. Is the channel-switching rate to be fixed or flexible? Continuous or interruptible? Should it be capable of stopping on one channel for test or calibration purposes?
- H. Is there danger of damage to active signal sources when the power is turned off? MOSFET multiplexers are inherently “safe” (at least in this sense), since the switches open when power is removed. JFET multiplexer switches can conduct when power is removed, making it possible to interconnect, and therefore damage, active signal sources.

#### *Sample-Holds*

- A. What is the input signal range? Gain?

- B. Considering the slewing rate of the signal and the multiplexer's channel-switching rate, what is the sample-hold's allowable acquisition time to within the desired error band?
- C. What accuracy is needed (gain, linearity, and offset errors)?
- D. What aperture delay and jitter are allowable, going into *hold* (The delay component of aperture time is considered to be correctible, since the switching operation can be advanced to compensate. The uncertainty (jitter) cannot be compensated, and a random jitter of 5ns applied to a signal slewing at, say, 1V/ $\mu$ s produces an uncertainty of 5mV. In sampled-data systems, operating at a constant sampling rate, with data that is not correlated to the sampling rate, delay is of no importance if fixed, but jitter modulates the sampling rate.
- E. How much droop is allowable in *hold*?
- F. What are the effects of time, temperature, and power supply variation?
- G. What offset error is caused by the flow of the sample-hold's input bias current through the series resistance of the multiplex switch and the signal source?

### 11.3 DEFINING THE SPECIFICATIONS

Figures 11.1 and 11.2 depict the specifications of typical d/a and a/d converters. Though the specs probably mean "what you think they mean," it is important that their meaning and implications be spelled out. The following list, in alphabetical order, should prove helpful. (Additional definitions will be found in Chapter 10 and in chapters on specific kinds of devices.)

*Accuracy, Absolute.* Absolute accuracy error of a *d/a converter* is the difference between actual analog output and the output that is expected when a given digital code is applied to the converter. Error is usually commensurate with resolution, i.e., less than  $2^{-(n+1)}$ , or " $\frac{1}{2}$  LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of  $\frac{1}{16}$ , but it might have an accuracy to within 0.01% of each ideal value.

Absolute accuracy error of an *a/d converter* at a given output code is the difference between the actual and the theoretical analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see *Quantizing Uncertainty*, and also Figure 7.2), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce that code. For example, if 5 volts,  $\pm 1.2$  mV, will theoretically produce a 12-bit half-scale code of 1000 0000 0000, then a converter for which any voltage from 4.997 V to 4.999 V will produce that code will have absolute error of  $(\frac{1}{2})(4.997 + 4.999) - 5$  volts = +2 millivolts.

Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Absolute accuracy measurements should be made under a set of

# SPECIFICATIONS

( $T_A = +25^\circ\text{C}$ ,  $\pm 12\text{V}$ ,  $\pm 15\text{V}$  power supplies unless otherwise noted)

Model	AD667J			AD667K			AD667S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>DIGITAL INPUTS</b>										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible, $T_{\min}$ – $T_{\max}$ ) <sup>1</sup>										
$V_{IH}$ (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
$V_{IL}$ (Logic "0")	0		+0.8	0		+0.8	0		+0.7	V
$I_{IH}$ ( $V_{IH} = 5.5\text{V}$ )		200	300		200	300		200	300	$\mu\text{A}$
$I_{IL}$ ( $V_{IL} = 0.8\text{V}$ )		50	100		50	100		50	100	$\mu\text{A}$
<b>TRANSFER CHARACTERISTICS</b>										
<b>ACCURACY</b>										
Linearity Error ( $\sigma$ + $25^\circ\text{C}$ )		$\pm 1/4$	$\pm 1/2$		$\pm 1/8$	$\pm 1/4$		$\pm 1/8$	$\pm 1/2$	LSB
$T_A = T_{\min}$ to $T_{\max}$		$\pm 1/2$	$\pm 3/4$		$\pm 1/4$	$\pm 1/2$		$\pm 1/2$	$\pm 3/4$	LSB
Differential Linearity Error ( $\sigma$ + $25^\circ\text{C}$ )		$\pm 1/2$	$\pm 3/4$		$\pm 1/4$	$\pm 1/2$		$\pm 1/4$	$\pm 3/4$	LSB
$T_A = T_{\min}$ to $T_{\max}$		<b>Monotonicity Guaranteed</b>			<b>Monotonicity Guaranteed</b>			<b>Monotonicity Guaranteed</b>		LSB
Gain Error <sup>2</sup>		$\pm 0.1$	$\pm 0.2$		$\pm 0.1$	$\pm 0.2$		$\pm 0.1$	$\pm 0.2$	%FSR <sup>3</sup>
Unipolar Offset Error <sup>2</sup>		$\pm 1$	$\pm 2$		$\pm 1$	$\pm 2$		$\pm 1$	$\pm 2$	LSB
Bipolar Zero <sup>2</sup>		$\pm 0.05$	$\pm 0.1$		$\pm 0.05$	$\pm 0.1$		$\pm 0.05$	$\pm 0.1$	% of FSR
<b>DRIFT</b>										
Differential Linearity		$\pm 2$			$\pm 2$			$\pm 2$		ppm of FSR/ $^\circ\text{C}$
Gain (Full Scale) $T_A = 25^\circ\text{C}$ to $T_{\min}$ or $T_{\max}$		$\pm 5$	$\pm 30$		$\pm 5$	$\pm 15$		$\pm 15$	$\pm 30$	ppm of FSR/ $^\circ\text{C}$
Unipolar Offset $T_A = 25^\circ\text{C}$ to $T_{\min}$ or $T_{\max}$		$\pm 1$	$\pm 3$		$\pm 1$	$\pm 3$		$\pm 1$	$\pm 3$	ppm of FSR/ $^\circ\text{C}$
Bipolar Zero $T_A = 25^\circ\text{C}$ to $T_{\min}$ or $T_{\max}$		$\pm 5$	$\pm 10$		$\pm 5$	$\pm 10$		$\pm 5$	$\pm 10$	ppm of FSR/ $^\circ\text{C}$
<b>CONVERSION SPEED</b>										
Settling Time to $\pm 0.01\%$ of FSR for FSR Change ( $2k\Omega$ /500pF load)										
with $10k\Omega$ Feedback		3	4		3	4		3	4	$\mu\text{s}$
with $5k\Omega$ Feedback		2	3		2	3		2	3	$\mu\text{s}$
For LSB Change		1			1			1		$\mu\text{s}$
Slew Rate	10			10			10			V/ $\mu\text{s}$
<b>ANALOG OUTPUT</b>										
Ranges <sup>4</sup>		$\pm 2.5$ , $\pm 5$ , $\pm 10$ , $+5$ , $+10$			$\pm 2.5$ , $\pm 5$ , $\pm 10$ , $+5$ , $+10$			$\pm 2.5$ , $\pm 5$ , $\pm 10$ , $+5$ , $+10$		V
Output Current	$\pm 5$			$\pm 5$			$\pm 5$			mA
Output Impedance (dc)		0.05			0.05			0.05		$\Omega$
Short Circuit Current			40			40			40	mA
<b>REFERENCE OUTPUT</b>										
External Current	9.90 0.1	10.00 1.0	10.10	9.90 0.1	10.00 1.0	10.10	9.90 0.1	10.00 1.0	10.10	V mA
<b>POWER SUPPLY SENSITIVITY</b>										
$V_{CC} = +11.4$ to $+16.5\text{V}$ dc		15	25		15	25		15	25	ppm of FS/%
$V_{EE} = -11.4$ to $-16.5\text{V}$ dc		3	10		3	10		3	10	ppm of FS/%
<b>POWER SUPPLY REQUIREMENTS</b>										
Rated Voltages		$\pm 12$ , $\pm 15$			$\pm 12$ , $\pm 15$			$\pm 12$ , $\pm 15$		V
Range <sup>4</sup>	$\pm 11.4$		$\pm 16.5$	$\pm 11.4$		$\pm 16.5$	$\pm 11.4$		$\pm 16.5$	V
Supply Drain										
+11.4 to +16.5V dc		5	8.5		5	8.5		5	8.5	mA
-11.4 to -16.5V dc		18	25		18	25		18	25	mA
<b>TEMPERATURE RANGE</b>										
Specification	0		+70	0		+70	-55		+125	$^\circ\text{C}$
Operating	-55		+125	-55		+125	-55		+125	$^\circ\text{C}$
Storage	-65		+125	-65		+125	-65		+150	$^\circ\text{C}$

## NOTES

<sup>1</sup>The digital input specifications are 100% tested at  $+25^\circ\text{C}$ , and guaranteed but not tested over the full temperature range.

<sup>2</sup>Adjustable to zero.

<sup>3</sup>FSR means "Full Scale Range" and is 20V for  $\pm 10\text{V}$  range and 10V for the  $\pm 5\text{V}$  range.

<sup>4</sup>A minimum power supply of  $\pm 12.5\text{V}$  is required for a  $\pm 10\text{V}$  full scale output and  $\pm 11.4\text{V}$  is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Figure 11.1. Typical microcircuit d/a converter specifications (AD667).

standard conditions with sources and meters traceable to an internationally accepted standard.

**Accuracy, Logarithmic DACs:** The difference (measured in dB) between the actual transfer function and the ideal transfer function, as measured after calibration of gain error at 0 dB.

**Accuracy, Relative.** Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to

## SPECIFICATIONS (typical @ +25°C with $V_{CC} = +15V$ or $+12V$ , $V_{LOGIC} = +5V$ , $V_{EE} = -15V$ or $-12V$ , unless otherwise specified)

Model	AD574AJ			AD574AK			AD574AL			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			12			12			12	Bits
LINEARITY ERROR 25°C (max) $T_{min}$ to $T_{max}$			$\pm 1$ $\pm 1$			$\pm 1/2$ $\pm 1/2$			$\pm 1/2$ $\pm 1$	LSB LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed) 25°C $T_{min}$ to $T_{max}$										Bits Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)			$\pm 2$			$\pm 2$			$\pm 2$	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)			$\pm 10$			$\pm 4$			$\pm 4$	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50 $\Omega$ resistor from REFOUT to REFIN) (Adjustable to zero) 25°C (max) $T_{min}$ to $T_{max}$ (Without Initial Adjustment) (With Initial Adjustment)			0.25 0.47 0.22			0.25 0.37 0.12			0.25 0.30 0.05	% of F.S. % of F.S. % of F.S.
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using internal reference) $T_{min}$ to $T_{max}$ Unipolar Offset  Bipolar Offset  Full Scale Calibration			$\pm 2$ 10 $\pm 2$ 10 $\pm 9$ 50			$\pm 1$ 5 $\pm 1$ 5 $\pm 5$ 27			$\pm 1$ 5 $\pm 1$ 5 $\pm 2$ 10	LSB ppm/°C LSB ppm/°C LSB ppm/°C
POWER SUPPLY REJECTION Max change in Full Scale Calibration $+13.5 \leq V_{CC} \leq +16.5V$ or $+11.4V \leq V_{CC} \leq +12.6V$ $+4.5 \leq V_{LOGIC} \leq +5.5V$ $-16.5 \leq V_{EE} \leq -13.5V$ or $-12.6V \leq V_{EE} \leq -11.4V$			$\pm 2$ $\pm 1/2$ $\pm 2$			$\pm 1$ $\pm 1/2$ $\pm 1$			$\pm 1$ $\pm 1/2$ $\pm 1$	LSB LSB LSB
ANALOG INPUT Input Ranges Bipolar  Unipolar  Input Impedance 10 Volt Span 20 Volt Span			-5 to +5 -10 to +10 0 to +10 0 to +20 3 6			-5 to +5 -10 to +10 0 to +10 0 to +20 3 6			-5 to +5 -10 to +10 0 to +10 0 to +20 3 6	Volts Volts Volts Volts k $\Omega$ k $\Omega$
POWER SUPPLIES Operating Range $V_{LOGIC}$ $V_{CC}$ $V_{EE}$ Operating Current $I_{LOGIC}$ $I_{CC}$ $V_{EE}$			+4.5 +11.4 -11.4 30 2 18			+5.5 +16.5 -16.5 40 5 30			+4.5 +11.4 -11.4 30 2 18	Volts Volts Volts mA mA mA
POWER DISSIPATION			390 725			390 725			390 725	mW
INTERNAL REFERENCE VOLTAGE Output current (available for external loads) (External load should not change during conversion)	9.9	10.0	10.1 1.5 <sup>1</sup>	9.9	10.0	10.1 1.5 <sup>1</sup>	9.9	10.0	10.1 1.5 <sup>1</sup>	Volts mA
PACKAGE OPTION (D28A)			AD574AJD			AD574AKD			AD574ALD	

### NOTES

<sup>1</sup>The reference should be buffered for operation on  $\pm 12V$  supplies.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Figure 11.2. Typical microcircuit a/d converter specifications (AD574A).

the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated (see *Full-Scale Range*; see also Chapter 10).

Since the discrete analog values that correspond to the digital values ideally lie on a straight line, the specified worst-case relative-accuracy error of a linear

ADC or DAC can be interpreted as a measure of end-point nonlinearity (see *Linearity*).

The “discrete points” of a D/A transfer characteristic are measured by the actual analog outputs. The “discrete points” of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see *Accuracy, Absolute*).

*Acquisition Time.* The acquisition time of a sample/track-hold circuit for a step change is the time required by the output to reach its final value, within a specified error band, after the sample (or track) command has been given. Included are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.

*Aperture (Delay) Time,* in a sample/track-hold, is the time required after the hold command, for the switch to open fully. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

*Aperture Uncertainty (or Jitter)* is the range of variation in the *aperture time*. If the *aperture time* is tuned out by advancing the *hold* command by a suitable amount—or if the signal is being sampled repetitively—this spec establishes the ultimate timing error, hence the maximum sampling frequency for a given resolution.

*Automatic Zero.* To achieve zero stability in many integrating-type converters, a time interval is provided during each conversion cycle to allow the circuitry to compensate for drift errors. The drift error in such converters is substantially zero.

*Bias Current* is the zero-signal dc current required from the signal source by the inputs of many semiconductor circuits. The voltage developed across the source resistance by bias current constitutes an (often negligible) offset error.

When an instrumentation amplifier performs measurements of a source that is disjoint from the amplifier’s power-supply, there *must* be a return path for bias currents. If it does not already exist and is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of “floating” sources, such as transformers, insulated thermocouples, and ac-coupled circuits, there must be a high-impedance dc leakage path from each input to common, or to the driven-guard terminal (if present). If a dc return path is impracticable, an *isolator* must be used.

*Bipolar Offset.* See *Offset*.

*Channel-to-Channel Isolation,* in multiple d/a converters. The proportion of analog input signal from one DAC’s reference input that appears at the output

of the other DAC, expressed logarithmically in dB. See also *crosstalk*.

**Character-Serial BCD.** Multiplexed BCD data outputs, where the 4-bit BCD code for each digit is gated in sequence onto four common output lines.

**Charge Transfer (or Offset Step),** the principal component of *sample-to-hold offset* (or *pedestal*) is the small charge transferred to the storage capacitor via interelectrode capacitance of the switch and stray capacitance when switching to the *hold* mode. The offset step is directly proportional to this charge, viz.,

$$\text{Offset error (volts)} = \frac{\Delta Q}{C} = \frac{\text{Incremental charge (picocoulombs)}}{\text{Capacitance (picofarads)}}$$

It can be reduced somewhat by lightly coupling an appropriate-polarity version of the *hold* signal to the capacitor for first-order cancellation. The error can also be reduced by increasing the capacitance, but this increases *acquisition time*.

**Code Width.** This is a fundamental quantity for a/d converter specifications. It is defined as the range of analog input values for which a given digital output code will occur (the stair treads in Figure 7.2). The nominal value of a code width (for all but the first and last codes) is the voltage equivalent of 1 least-significant bit (LSB) of the full-scale range, or 2.44 mV out of 10 volts for a 12-bit ADC. Noise modulates (and narrows) the effective code width. Code width should generally not be less than  $\frac{1}{2}$  LSB or more than  $1\frac{1}{2}$  LSB. Because the full-scale range is fixed, the presence of excessively wide codes implies the existence of narrow—and perhaps even missing—codes.

**Common-Mode Range.** Common-mode rejection usually varies with the magnitude of the range through which the input signal can swing, determined by the sum of the common-mode and the differential voltage. *Common-mode range* is that range of *total* input voltage over which specified common-mode rejection is maintained. For example, if the common-mode signal is  $\pm 5\text{V}$  and the differential signal is  $\pm 5\text{V}$ , the common-mode range is  $\pm 10\text{V}$ .

**Common-Mode Rejection (CMR)** is a measure of the change in output voltage when both inputs are changed by equal amounts of ac and/or dc voltage. Common-mode rejection is usually expressed either as a ratio (e.g.,  $\text{CMRR} = 1,000,000:1$ ) or in decibels:  $\text{CMR} = 20 \log_{10} \text{CMRR}$ ; if  $\text{CMRR} = 10^6$ ,  $\text{CMR} = 120 \text{ dB}$ . A CMRR of  $10^6$  means that 1 volt of common mode is processed by the device as though it were a differential signal of 1-microvolt at the input.

CMR is usually specified for a full-range common-mode voltage change (CMV), at a given frequency, and a specified imbalance of source impedance (e.g., 1 k $\Omega$  source unbalance, at 60 Hz). In amplifiers, the common-mode rejection ratio is defined as the ratio of the signal gain,  $G$ , to the common-mode gain (the ratio of common-mode signal appearing at the output to the CMV at the input).

*Common-Mode Voltage (CMV).* A voltage that appears in common at both input terminals of a device, with respect to its output reference (usually “ground”). For inputs,  $V_1$  and  $V_2$ , with respect to ground,  $CMV = \frac{1}{2}(V_1 + V_2)$ . An ideal differential-input device would ignore CMV. *Common-mode error (CME)* is any error at the output due to the common-mode input voltage. The errors due to supply-voltage variation, an internal common-mode effect, are specified separately.

In *isolation amplifiers*, the rating, *CMV, inputs to outputs*, is the voltage that may be safely applied to *both* inputs, with respect to the outputs or power common. This is a necessary consideration in applications with high CMV input or when high voltage-transients may occur at the input.

*Compliance-Voltage Range.* For a current source (e.g., a current-output DAC), the maximum range of (output) terminal voltage for which the device will maintain the specified current-output characteristics.

*Conversion Time and Conversion Rate.* The time required for a complete measurement by an analog-to-digital converter is called *conversion time*. For most converters (assuming no significant additional systemic delays), conversion time is essentially identical with the inverse of *conversion rate*. However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined; thus, for example, the Analog Devices MOD-1205 can provide 12-bit output data at a 5-MHz word rate (200 ns/conversion), even though the time for any one conversion, from start to finish, is two clock periods plus 275 ns, or 675 ns, at 5 MHz.

In digital panel instruments, *conversion rate* is the frequency at which readings may be processed by the instrument. Specifications are typically given for internally clocked rates and maximum permissible externally triggered rates. *Conversion time* is the maximum time required for the instrument to complete a reading cycle—it is specified for the full-scale reading

*Crosstalk.* Leakage of signals, usually via capacitance between circuits or channels of a multi-channel system or device, such as a multiplexer, multiple op amp, or multiple DAC. Crosstalk is usually determined by the impedance parameters of the physical circuit, and actual values are frequency-dependent. See also *channel-to-channel isolation*.

Multiple d/a converters have a *digital crosstalk* specification: the spike (sometimes called glitch) impulse appearing at the output of one converter due to a change in the digital input code of another of the converters. It is specified in nanovolt-seconds and measured at  $V_{REF} = 0$  V.

*Deglitcher (See Glitch).* A device that removes or reduces the effects of time-skew pulses in d/a conversion. A deglitcher normally employs a sample-hold circuit, often specifically designed as part of the DAC. When the DAC is up-

dated, the deglitcher holds the output of the DAC's output amplifier constant at the previous value until the switches reach equilibrium, then samples and holds the new value.

*Digital-to-Analog Spike (also Glitch) Impulse.* For CMOS multiplying DACs, this is a measure of the charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified in terms of the area of the spike in nanovolt-seconds, and is measured with  $V_{REF}$  at analog ground and a fast operational amplifier as the output amplifier.

*Droop Rate.* When a sample-and-hold circuit using a capacitor for storage is in *hold*, it will not hold the information forever. Droop rate is the rate at which the output voltage changes (by increasing or decreasing), and hence gives up information. The change of output occurs as a result of leakage or bias currents flowing through the storage capacitor. The polarity of change depends on the sources of leakage within a given device. In integrated circuits with external capacitors, it is usually specified as a (*droop* or *drift*) current, in modules or ICs having internal capacitors, a rate of change. Note:  $dV/dt$  (volts/second) =  $I/C$  (picoamperes/picofarads).

*Dual-Slope Converter.* An integrating A/D converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally.

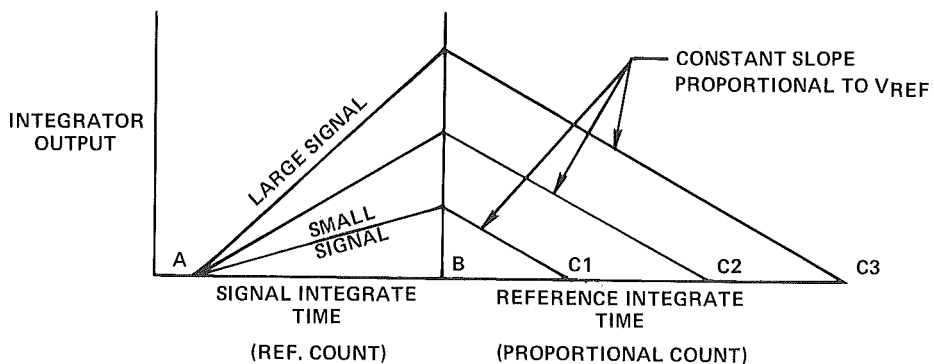


Figure 11.3. Voltage-time relationships in dual-slope conversion.

This is done by integrating the unknown for a predetermined length of time. Then a reference input is switched to the integrator, which integrates “down” from the level determined by the unknown until the starting level is reached. The time for the second integration process, as determined by the counter, is proportional to the average of the unknown signal level over the predetermined integrating period. The counter provides the digital readout.



*Feedthrough.* Undesirable signal-coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a sample-and-hold, multiplexer, or multiplying DAC. Feedthrough is variously specified in percent, parts per million, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

In a multiplying DAC, *feedthrough* error is caused by capacitive coupling from an ac  $V_{REF}$  to the output, with all switches off. In a sample-and-hold, *feedthrough* is the fraction of the input signal variation or ac input waveform that appears at the output in *hold*. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

*“Flash” Converter.* A converter in which all the bit choices are made at the same time. It requires  $2^n - 1$  voltage-divider taps and comparators—and a comparable amount of priority encoding logic. A scheme that gives extremely fast conversion, it requires large numbers of nearly identical components, hence it is well-suited to—and really only feasible in—integrated-circuit form. Flash converters are often used in pairs for two-stage conversion in *sub-ranging converters*, to provide high resolution at somewhat slower speed than pure flash conversion.

*Four-Quadrant.* In a multiplying DAC, “four quadrant” refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. Such a DAC can be thought of as a gain control for ac signals (“reference” input) with a range of positive and negative digitally controlled gains. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign.

*Frequency-to-Voltage Conversion (FVC).* The input of a FVC device is an ac waveform—usually a train of pulses (in the context of conversion); the output is an analog voltage, proportional to the number of pulses occurring in a given time. FVC is usually performed by a voltage-to-frequency converter in a feedback loop. Important specifications, in addition to the accuracy specs typical of VFCs (see *Voltage-to-Frequency conversion*), include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated, and for versatility in interfacing several types of sensors directly), *hysteresis*, to provide a degree of insensitivity to noise superimposed on a slowly varying input waveform, and *dynamic response* (important in motor control).

*Full-Scale Range (FSR).* For binary ADCs and DACs, that magnitude of voltage, current, or—in a multiplying DAC—gain, of which the MSB is specified to be exactly one-half—or for which any bit or combination of bits is tested against its (their) prescribed ideal ratio(s). FSR is independent of resolution; the value of the LSB (voltage, current, or gain) is  $2^{-n}$  FSR.

There are several other terms, with differing meanings, that are often used

in the context of discussions or operations involving full-scale range. They are:

*Full Scale*—similar to full-scale range, but pertaining to a single polarity. Thus, full-scale for a unipolar device is twice the prescribed value of the MSB and has the same polarity. For a bipolar device, *positive or negative full scale* is that positive or negative value, of which the next bit after the polarity bit is tested to be one-half.

*Span*—the scalar voltage or current range corresponding to FSR.

*All-1's*—*All bits on*, the condition used, in conjunction with *all-zeros*, for gain adjustment of an ADC or DAC, in accordance with the manufacturer's instructions. Its magnitude, for a binary device, is  $(1 - 2^{-n})$  FSR. *All-1's* is a *positive-true* definition of a specific magnitude relationship; for complementary coding the "all-1's" code will actually be all zeros. To avoid confusion, all-1's should never be called "full scale;" FSR and FS are independent of the number of bits, all-1's isn't.

*All-0's*—*All bits off*, the condition used in offset (and gain) adjustment of a DAC or ADC, according to the manufacturer's instructions. All-0's corresponds to zero output in a unipolar DAC and negative full-scale in an offset bipolar DAC with positive output reference. In a sign-magnitude device, all-0's refers to all bits after the sign bit. Analogous to "all-1's," "all-0's" is a *positive-true* definition of the *all-bits-off* condition; in a complementary-coded device, it is expressed by all ones. To avoid confusion, all-0's should not be called "zero" unless it accurately corresponds to true analog zero output from a DAC.

The best way of defining the critical points for an actual device is a brief table of critical codes and the ideal voltages, currents, or gains to which they correspond, with the conditions for measurement defined.

*Gain*. The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10 volts full-scale. In a multiplying DAC or ratiometric ADC, it is indeed a gain. In a device with fixed internal reference, it is expressed as the full-scale magnitude of the output parameter (e.g., 10 volts or 2 milliamperes). In a fixed-reference converter, where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain and zero adjustment are discussed under *zero*.

"*Glitch*" (see Figure 11.4). Transients associated with code changes generally stem from several sources. Some are spikes, known as digital-to-analog feed-through, or charge transfer, coupled from the digital signal to the analog output, defined with zero reference. These spikes are generally fast, fairly uniform, code-independent, and hence filterable. However, there is a more-insidious form of transient, code-dependent, and difficult to filter, known as the "glitch."

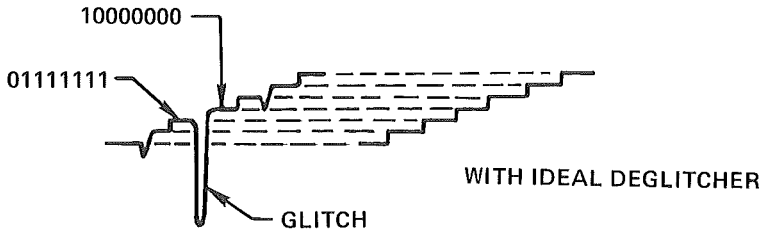


Figure 11.4. Glitch at a major carry.

If the output of a counter is applied to the input of a DAC to develop a “staircase” voltage, the number of bits involved in a code change between two adjacent codes establish “major” and “minor” transitions. The most major transition is at  $\frac{1}{2}$ -scale, when the D/A switches all bits, i.e., from 011. . .111 to 1000. . .00. If, for digital inputs having no skew, the switches are faster to switch *off* than *on*, this means that, for a short time, the DAC will seek zero output, and then return to the required 1 LSB above the previous reading. This large transient spike is commonly known as a “glitch.” The better-matched the input transitions and the switching times, the faster the switches, the smaller will be the energy contained in the glitch. Because the size of the glitch is not proportional to the signal change, linear filtering may be unsuccessful and may, in fact, make matters worse. (See also *Deglitcher*.)

The severity of a glitch is specified by *glitch impulse*, the product of its duration and its average magnitude, i.e., the net area under the curve. This product will be recognized as the physical quantity, *impulse* (electromotive force  $\times$   $\Delta$ time); however, it has also been termed “glitch energy” and “glitch charge.” Glitch impulse is usually expressed, for fast converters, in units of picovolt-seconds (equivalent to the more-readily visualized millivolt-nanoseconds).

The glitch can be minimized through the use of fast, non-saturating logic, such as ECL, matched latches, and non-saturating switches. Very fast DACs, such as those used in high-resolution raster-type displays, often include arrangements for trimming the glitch to take the form of a small, filterable doublet pulse, which has near-zero net area and a doubled fundamental frequency (see Section 13.2.1).

*Glitch Charge, Glitch Energy, Glitch Impulse. See Glitch.*

**Leakage Current, Output.** Current which appears at the output terminal of a d/a converter with all bits “off.” For a converter with two complementary outputs (for example, some CMOS DACs), output leakage current is the current measured at OUT 1, with all digital inputs *low*—and the current measured at OUT 2, with all digital inputs *high*.

**Least-Significant Bit (LSB).** In a system in which a numerical magnitude is represented by a series of binary (i.e. two-valued) digits, the *least-significant*

*bit* is that digit (or “bit”) that carries the smallest value, or weight. For example, in the natural binary number 1101 (decimal 13, or  $(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (2^0)$ ), the rightmost digit is the LSB. Its analog weight, in relation to full scale (see *Full-Scale Range*), is  $2^{-n}$ , where  $n$  is the number of binary digits. It represents the smallest analog change that can be resolved by an  $n$ -bit converter.

In converter nomenclature (viz., fractional binary), the LSB is bit  $n$ ; in bus nomenclature (integer binary), it is Data Bit 0.

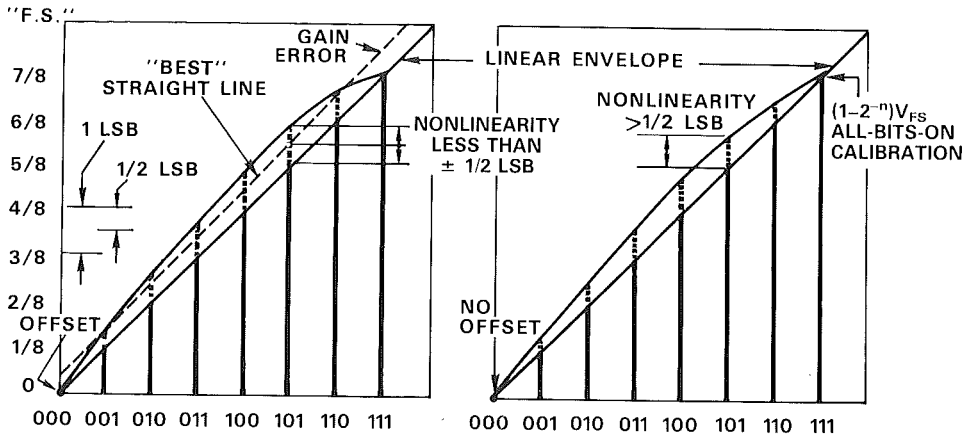
*Linearity.* (See also *Nonlinearity*.) Linearity error of a converter (also, *integral nonlinearity*—see *Linearity, Differential*), expressed in % or parts per million of full-scale range, or (sub)multiples of 1 LSB, is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a “best straight line,” determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated, sometimes referred to as “end-point” linearity (Figure 11.5). “End-point” nonlinearity is similar to relative accuracy error (see *Accuracy, Relative*). It provides an easier method for users to calibrate a device, and it is a more conservative way to specify linearity.

For multiplying D/A converters, the *analog* linearity error, at a specified analog gain (digital code), is defined in the same way as for analog multipliers, i.e., by deviation from a “best straight line” through the plot of the analog output-input response.

*Linearity, Differential.* In a d/a converter, any two adjacent digital codes should result in measured output values that are exactly 1 LSB apart ( $2^{-n}$  of full scale for an  $n$ -bit converter). Any positive or negative deviation of the measured “step” from the ideal difference is called *differential nonlinearity*, expressed in (sub)multiples of 1 LSB. It is an important specification, because a differential linearity error more negative than  $-1$  LSB can lead to non-monotonic response in a d/a converter and missed codes in an a/d converter using that DAC.

Similarly, in an a/d converter, midpoints between code transitions should be 1 LSB apart. Differential nonlinearity is the deviation between the actual difference between midpoints and 1 LSB, for adjacent codes. If this deviation is equal to or more negative than  $-1$  LSB, a code will be missed, as shown in Figure 7.2.

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of “monotonicity” or “no missing codes”, which implies that the differential nonlinearity cannot be more negative than  $-1$  for any adjacent pair of codes. However, the differential linearity error may still be somewhere more positive than  $+1$  LSB.



a.  $1/2$ -LSB nonlinearity achieved by arbitrary location of "best straight line."

b. Nonlinearity reference is straight line through end points.  $1/2$ -LSB nonlinearity error is half that of (a).

Figure 11.5. Comparison of linearity criteria for 3-bit d/a converter. Straight line through end points is easier to measure and provides a more-conservative specification.

**Linearity, Integral.** See *Linearity*. While *differential linearity* deals with errors in step size, *integral linearity* has to do with deviations of the overall shape of the conversion response. Even converters that are not subject to differential-linearity errors (e.g., integrating types) have integral-linearity (sometimes just "linearity") errors.

**Missing Codes.** An a/d converter is said to have missing codes when a transition from one quantum of the analog range to the adjacent one does not result in the adjacent digital code, but in a code removed by one or more counts. Missing codes can be caused by large negative differential-linearity errors, noise, or changing inputs during conversion. A converter's proclivity towards missing codes is also a function of temperature.

**Monotonicity.** A DAC is said to be *monotonic* if its output either increases or remains constant as the digital input increases, with the result that the output will always be a single-valued function of the input. The condition "monotonic" requires that the derivative of the transfer function never change sign. Monotonic behavior requires that the differential nonlinearity be more positive than  $-1$  LSB.

**Most Significant Bit (MSB).** In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the *most-significant bit* is that digit (or "bit") that carries the greatest value or weight. For example, in the natural binary number 1101 (decimal 13, or  $(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$ ), the leftmost "1" is the MSB, with a weight of  $1/2$  nominal

peak-to-peak full scale (full-scale range). In bipolar devices, the sign bit is the MSB. In A/D converters having overrange bits, the MSB is the most-significant “overrange” bit.

In converter nomenclature (viz., fractional binary), the MSB is bit 1; in bus nomenclature (integer binary), it is Data Bit ( $n - 1$ ).

*Multiplying DAC.* A multiplying DAC differs from the conventional fixed-reference DAC in being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the “reference” (i.e., analog input) voltage and the fractional equivalent of the digital input number. See also *Four-Quadrant*.

*Noise, Peak and RMS.* Internally generated random noise is not a major factor in d/a converters, except at extreme resolutions and dynamic ranges. Random noise is characterized by rms specifications for a given bandwidth, or as a spectral density (current or voltage per root hertz); if the distribution is Gaussian, the probability of peak-to-peak values exceeding  $7 \times$  the rms value is less than 0.1%.

Of much greater importance in DACs is interference, in the form of high-amplitude, low-energy (hence low-rms) spikes appearing at a DAC's output, caused by coupling of digital signals in a surprising variety of ways; they include coupling via stray capacitance, via power supplies, via inadequate ground systems, via feedthrough, and by glitch-generation (see *Glitch*). Their presence underscores the necessity for maximum application of the designer's art, including layout, shielding, guarding, grounding, bypassing, and deglitching.

Noise in a/d converters in effect narrows the region between transitions and can cause missing codes in a converter with marginal differential nonlinearity. Sources of noise include the comparator, the reference, the analog signal itself, and pickup in infinite variety.

*Nonlinearity*—or “gain nonlinearity”—in an instrumentation or isolation amplifier is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a “best straight line,” with the output swinging through its full-scale range. Nonlinearity is usually specified in percent of full-scale output range.

*Normal Mode.* For an amplifier used in instrumentation, the *normal-mode* signal is the actual difference signal being measured. This signal often has noise associated with it. Signal-conditioning systems and digital panel instruments usually contain input filtering to remove high-frequency—and line-frequency—noise components. *Normal-mode rejection* (NMR), is a logarithmic measure of the attenuation of normal-mode noise components at specified frequencies in dB.

*Offset, Bipolar.* For the great majority of bipolar converters (e.g.,  $\pm 10$ -volt output), negative currents are not actually generated to correspond to negative numbers; instead, a unipolar DAC is used, and the output is offset by half full scale (1 MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

Because of nonlinearity, a device with perfectly calibrated end points may have offset error at analog zero.

*Offset Step.* See *Pedestal*.

*Output Voltage Tolerance.* For a reference, the maximum deviation from the nominal output voltage at 25°C and specified input voltage, as measured by a device traceable to a recognized fundamental voltage standard.

*Overload (Digital Panel Instruments).* An input voltage exceeding the instrument's full-scale range produces an overload condition, usually indicated by conspicuous manipulation of the display, such as all dashes, flashing zeros, etc. On a  $3\frac{1}{2}$ -digit DPM with a range of 199.9 mV, a signal exceeding 200 mV will produce an overload condition.

*Overrange (Digital Panel Instruments).* An input signal that exceeds all nines on a DPM, but is less than an overload. On a  $3\frac{1}{2}$ -digit DPM with a full-scale range of 199.9 mV, the all-nines range is 0 to 99.9 mV, and signals from 100 to 199.9 mV are said to fall in the 100% overrange region. Some panel meters have higher overrange capability; a  $3\frac{3}{4}$ -digit meter has a full-scale range of 3.999, or 300% overrange.

*Pedestal, or Sample-to-Hold Offset Step.* In sample/track-hold amplifiers, a shift in level between the last value in *sample* and the value settled-to in *hold*; in devices having fixed internal capacitors, it includes *charge transfer*, or *offset step*. However, for devices that may use external capacitors, it is often defined as the residual step error after the *charge transfer* is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as *offset nonlinearity*.

*Power-Supply Rejection Ratio (PSRR).* The ratio of a change in dc power-supply voltage to the resulting change in the specified device error, expressed in percentage, parts per million, or fractions of 1 LSB. It may also be expressed logarithmically, in dB ( $PSR = 20 \log_{10}(PSRR)$ ).

*Power-Supply Sensitivity.* The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog value—or fractions of 1 LSB — (D/A output, A/D input) for a 1% dc change in the power supply, e.g.,  $0.05\%/ \% \Delta V_s$ . Power-supply sensitivity may also be expressed in relation to a specified maximum dc shift

of power-supply voltage. A converter may be considered “good” if the change in reading at full scale does not exceed  $\pm \frac{1}{2}$ -LSB for a 3% change in power-supply voltage. Even better specs are necessary for converters designed for battery operation.

*Propagation Delay.* In CMOS DACs, a measure of the internal delays of the circuit, propagation delay is defined as the time from a digital input change to the time at which the analog output current reaches 90% of its final value.

*Quad-Slope Converter.* This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme can result in high-accuracy conversion.

*Quantizing Uncertainty (or “Error”).* The analog continuum is partitioned into  $2^n$  discrete ranges for  $n$ -bit conversion and processing. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal mid-range value. There is, therefore, an inherent quantization uncertainty of  $\pm \frac{1}{2}$  LSB, in addition to the actual conversion errors. In integrating a/d converters, this “error” is often expressed as “ $\pm 1$  count.” Depending on the system context, it may be interpreted as a truncation (round-off) error or as noise.

*Ratiometric.* The output of an a/d converter is a digital number proportional to the *ratio* of (some measure of) the input to a reference voltage. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference; but this presumes that the signal applied to the converter is either reference-independent or in some way derived from another fixed reference. However, real references are not truly fixed; the references for both the converter and the signal source vary with time, temperature, loading, etc. Therefore, if the converter is used with signal sources that also rely on references (for example, strain-gage bridges, RTDs, thermistors), it makes sense to replace this multiplicity of references by a single system reference; reference-caused errors will tend to cancel out. This can be done by using the converter’s internal reference (if it has one) as the system reference. Another way is to use a separate external system reference, which also becomes the reference for a *ratiometric* converter.

Over limited ranges, ratiometric conversion can also serve as a substitute for analog or digital signal division (where the denominator changes by less than  $\frac{1}{2}$  LSB during the conversion). The signal input is the numerator; the reference input is the denominator.

*Resolution.* An  $n$ -bit binary converter should be able to provide  $2^n$  distinct and different analog output values corresponding to the set of  $n$ -bit binary words. A converter that satisfies this criterion is said to have a *resolution* of  $n$  bits.



The smallest output change that can be resolved by a linear DAC is  $2^{-n}$  of the full-scale span. Thus, for example, the resolution of an 8-bit DAC would be  $2^{-8}$ , or  $1/256$ . On the other hand, a nonlinear device, such as the AD7111 LOG-DAC<sup>TM</sup>,\* can ideally achieve a dynamic range of 89.625 dB, or 30,000:1, in 0.375-dB steps, using only 8 bits of digital resolution.

For digital panel instruments, *resolution* is the smallest voltage increment that can be measured. It is a function of full-scale range and the number of digits. For example, if a 3 1/2-digit DPM has a resolution of 1 part in 2,000 (0.05%) over a full-scale range of 199.9 mV, the DPM can resolve 0.1 mV.

*Sample-to-Hold Offset.* See *Pedestal*.

**Settling Time—Amplifier.** Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from the slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a “long tail” due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (i.e., an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably—but not always—be expected to have fast settling), settling time cannot usually be predicted from the other dynamic specifications.

**Settling Time—DAC.** The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually  $\pm 1/2$  LSB) of the final value. Typical prescribed changes are full-scale, 1 MSB, and 1 LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of an output op-amp chip.

**Single-Slope Conversion.** In the single-slope converter, a reference voltage is integrated until the output of the integrator is equal to the input voltage. The time period required for the integrator to go from zero to the level of the input is proportional to the magnitude of the input voltage and is measured by an internal clock. Measurement accuracy is sensitive to clock speed and integrating capacitance, as well as the reference accuracy.

\*LOGDAC is a trade mark of Analog Devices, Inc.

*Slew(ing) Rate.* A limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate greater than about 75 volts/microsecond are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output d/a converter is usually limited by the slew rate of the amplifier used at its output.

*Stability.* In a well-designed, intelligently applied converter, *dynamic stability* is not an important question. The term stability usually applies to the insensitivity of the converter's characteristics to time, temperature, etc. All measurements of stability are difficult and time-consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see *Temperature Coefficient*).

*Staircase.* A voltage or current, increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot); it is generated by applying a pulse train to a counter, and the output of the counter to the input of a DAC.

A very simple a/d converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1 LSB, the count is stopped, and the code corresponding to the count is the digital input. If the counter is an up/down counter, where up/down is controlled by the comparator state, with correct polarity, the converter will tend to track the input signal.

*Subranging A/D Converters.* In this type of converter, an extremely fast—i.e., *flash*—conversion produces the most-significant portion of the output word. This portion is stored in a holding register and also converted back to analog with a fast, high-accuracy d/a converter. The analog result is subtracted from the input, and the resulting residue is amplified, converted to digital at high speed, and combined with the results of the earlier conversion to form the output word. In *digitally corrected subranging* (DCS), the two bytes are combined in a manner that corrects for the error of the LSB of the most-significant byte. For example, using 8-bit and 5-bit conversion, plus this technique and a great deal of video-speed converter expertise, a full-accuracy high-speed 12-bit converter can be built.

*Successive Approximations.* Successive approximations is a high-speed method of conversion by comparing an unknown against a group of weighted references. The operation of a successive-approximation a/d converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights, such as 1 gram  $\frac{1}{2}$  gram,  $\frac{1}{4}$  gram, etc. The weights are tried in order, starting with the largest. Any weight that tips the scale is removed. At the end of the process, the sum of the weights remaining

on the scale will be within 1 LSB of the actual weight ( $\pm \frac{1}{2}$  LSB, if the scale is properly biased—see Zero).

*Switching Time.* In a d/a converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time.

*Temperature Coefficient.* In general, temperature instabilities are expressed as  $\%/^{\circ}\text{C}$ ,  $\text{ppm}/^{\circ}\text{C}$ , fractions of 1 LSB per degree C., or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include gain, linearity, offset (bipolar), and zero.

a. *Gain Tempco:* Two factors principally affect converter gain stability with temperature. In fixed-reference converters, the reference voltage will vary with temperature (generally less than 5 ppm/ $^{\circ}\text{C}$  for the AD581L). The reference circuitry and switches (and comparator in a/d converters) will add a few more ppm/ $^{\circ}\text{C}$ .

b. *Linearity Tempco:* Sensitivity of linearity (integral and/or differential linearity) to temperature, in  $\% \text{FSR}/^{\circ}\text{C}$  or ppm FSR/ $^{\circ}\text{C}$ , over the specified range. Monotonic behavior in DACs is achieved if the differential nonlinearity is less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range, and/or implied by a statement that the device is monotonic over the specified temperature range. To avoid missing codes in noiseless a/d converters, it is sufficient that the differential nonlinearity error magnitude be less than 1 LSB at any temperature in the range of interest. The temperature coefficient is often implied by the statement that there are no missed codes when operating within a specified temperature range.

c. *Zero TC (unipolar converters):* The temperature stability of a unipolar fixed-reference DAC, measured in  $\% \text{FSR}/^{\circ}\text{C}$  or ppm FSR/ $^{\circ}\text{C}$ , is principally affected by current leakage (current-output DAC), and offset voltage and bias current of the output op amp (voltage-output DAC). The zero stability of an ADC is dependent on the zero stability of the DAC or integrator and/or the input buffer and the comparator. It is expressed in  $\mu\text{V}/^{\circ}\text{C}$  or in percent or ppm of full-scale range (FSR) per degree C.

d. *Offset Tempco:* The temperature coefficient of the all-DAC-switches-off (minus full-scale) point of a bipolar converter (in  $\% \text{FSR}/^{\circ}\text{C}$  or ppm FSR/ $^{\circ}\text{C}$ ) depends on three major factors—the tempco of the reference source, the voltage zero-stability of the output amplifier, and the tracking capability of the bipolar-offset resistors and the gain resistors. In an a/d converter, the

corresponding tempco of the negative full-scale point depends on similar quantities—the tempco of the reference source, the voltage stability of the input buffer and the comparator, and the tracking capabilities of the bipolar offset resistors and the gain resistors.

*Thermal Tail.* The slow drift of an amplifier having a thermally induced offset due to self-heating as it settles to a final electrical equilibrium value corresponding to internal thermal equilibrium.

*Total Unadjusted Error.* A comprehensive specification on some devices which includes full-scale error, relative-accuracy and zero-code errors, under a specified set of conditions.

*Zero- and Gain-Adjustment Principles.* (This is not a substitute for the manufacturer's instructions, which should be followed in detail.)

a. *DACs:* The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for F.S.  $(1 - 2^{-n})$  with all bits on. The “zero” of an offset-binary bipolar DAC is set to  $-F.S.$  with all bits off, and the gain is set for  $+F.S. (1 - 2^{-(n-1)})$  with all bits on.

b. *ADCs:* The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at  $\frac{1}{2} (2^{-n}) F.S.$  The gain is set for the final transition to all-bits-on at F.S.  $(1 - 3/2 \cdot 2^{-n})$ . The “zero” of an offset-binary bipolar ADC is set so that the first transition occurs at  $-F.S. (1 - 2^{-n})$  and the last transition at  $+F.S. (1 - 3 \times 2^{-n})$ .

## 11.4 SYSTEM-COMPONENT SELECTION PROCESS

The most natural process for selection of appropriate off-the-shelf components to meet a system requirement involves a method of “successive approximations:” Choose the least costly device that meets the most significant requirements, and perform an error analysis to check its adequacy.

If its performance seems far better than that needed for the other requirements (at possibly excessive cost), or inadequate in some respects, inspect the discrepancies for possible design tradeoffs, make a new choice (if necessary) and repeat the analysis. Remember, though, that in a maturing industry, costs can be expected to decline. *It is often less costly, in the long run, to go for better performance (rather than lowest possible cost) in the initial stages of a design.* Also, efforts aimed at reducing the cost of any element of a system should bear in mind the criticality of that element and the relationship of its cost relative to that of the entire project.

Where new designs are concerned and early results are essential, unless one is an experienced system designer with plenty of component and manufacturing experience (if quantities are involved), it is usually good judgement to ignore initial cost (within the limits of good sense) and go for performance, con-

venience, and the highest level of system integration that the budget will allow (see Chapter 4).

## 11.5 EXAMPLE OF A SELECTION AND VERIFICATION PROCESS\*

A computer data-acquisition system is to be assembled to process data from a number of strain gages. Signal-conditioning hardware, to be purchased with the gages, delivers  $\pm 10\text{V}$  full-scale signals with 10-ohm source impedance. The signal channels must be sequentially scanned in no more than 50 microseconds per channel. Maximum allowable error of the system is about 0.1% of full scale. System logic is to be TTL, and hardware may work in either binary or 2's complement code. Parallel data readout will be used.

Probable temperature range in the equipment cabinets (including equipment temperature rise) is  $+25^{\circ}\text{C}$  to  $+55^{\circ}\text{C}$ . Sufficient power at both  $\pm 15\text{V}$  and  $+5\text{V}$  is available, but the regulation of the  $\pm 15\text{V}$  supply is 150mV.

The objective: specify a set of conversion components having appropriate accuracy and speed.

### 11.5.1 FIRST APPROXIMATION

A useful rule of thumb that usually provides satisfactory results is this: For the critical specs of a multi-component system, choose each component to perform roughly 10 times better than the overall desired performance. Thus, for a system that needs 0.1%-grade performance, use a 0.01% converter (12 bits) with a compatible multiplexer and sample-hold amplifier.

Reviewing the available a/d converter ICs, we find AD574A to be a possible choice; it completes a conversion in  $25\mu\text{s}$ . For a sample-hold, the compatible AD585 is chosen, adding  $0.5\mu\text{s}$  of settling time. Thus, the combination appears to be amply capable of meeting the  $50\mu\text{s}/\text{channel}$  scanning requirement. Since the multiplexer will scan sequentially, its settling time is unimportant. The multiplexer can be switched to the next address as soon as the SHA goes into *hold* on data from the current address. Thus it has at least  $25\mu\text{s}$  to settle before a measurement is called for. For convenience and small size, one should consider the AD7501 CMOS 8-channel multiplexer.

### 11.5.2 ERROR ANALYSIS

It's clear that the AD7501, the AD585, and the AD574A generally meet the problem's requirements. Now we must look further into the details of errors, to determine if the worst-case situation is within the allowable 0.1% system error.

\*For maximum tutorial benefit, to avoid clutter, and to fit the available space, some of the known but less-salient sources of error have been intentionally omitted. For any that readers are concerned about for particular applications but don't see treated here, it is worth noting that most converter manufacturers, including Analog Devices, make available competent applications engineers who can be reached by mail or by telephone.

### Multiplexer

The switches of the AD7501, being MOSFET's, with variable-resistance channels, are not subject to voltage offset errors. Errors here will be due on two factors:

1. Leakage current into the *on* channel from the *off* channels develops an offset voltage across the source impedance.

$$\begin{aligned} \text{Leakage current @ } 25^{\circ}\text{C} & 10 \text{ nA} \\ \text{Source impedance} & 10 \text{ ohms} \\ \text{Error voltage} & = 10 \times 10 \times 10^{-9} = 10^{-7} \text{ V (0.01 ppm, negligible)} \end{aligned}$$

2. Transfer error due to voltage division across the MOSFET *on* resistance and input impedance of the sample-hold amplifier (AD585):

$$\begin{aligned} \text{ON resistance} & 300 \text{ ohms maximum} \\ \text{AD585 } R_{\text{in}} & 10^{12} \text{ ohms} \\ \text{Divider ratio attenuation error: } & 3 \times 10^{-10} \text{ (0.0003 ppm, negligible)} \end{aligned}$$

### Sample-Hold

1. Nonlinearity is 2mV over the 20V range, or 0.01% . . . . . 100 ppm
2. Gain error of 0.01% maximum (and other similarly small initial gain errors in the system) may be compensated for overall performance when calibrating

Resolution	Family	Output Type	Bus Interface	Reference	Conversion Time	Comments
8 Bits	AD570	3-state buffer	TTL-compatible	Internal	20 $\mu$ s	Instr. amp. input
	AD670	3-state buffer	TTL-compatible	Internal	10 $\mu$ s	
	AD673	3-state buffer	TTL-compatible	Internal	20 $\mu$ s	
	AD7574	3-state buffer	TTL-compatible	External	15 $\mu$ s	CMOS
	AD7576	3-state buffer	TTL-compatible	External	10 $\mu$ s	CMOS
	AD7581	3-state buffer	TTL-compatible	External	Continuous	8-Channel memory
	AD7820	3-state buffer	TTL-compatible	External	1.5 $\mu$ s	CMOS on-board S/H
10 Bits	AD579	Binary	TTL-compatible	Internal	1.8 $\mu$ s	Hybrid
	AD573	Binary	TTL-compatible	Internal	20 $\mu$ s	CMOS
	AD7571	3-state buffer	CMOS-compatible	External	80 $\mu$ s	
12 Bits	AD574A	3-state buffer	TTL-compatible	Internal	25 $\mu$ s	Hybrid Hybrid
	AD578	Binary	TTL-compatible	Internal	3 $\mu$ s	
	AD ADC80	Ser/Par bin.	TTL-compatible	Internal	25 $\mu$ s	CMOS 4-channel MUX
	AD7582	4-8 latch 3-state buffer	TTL-compatible	External	100 $\mu$ s	
16 Bits	AD ADC71	Ser/Par bin.	TTL-compatible	Internal	45 $\mu$ s	Hybrid

Table 11.1. General-Purpose Analog-to-Digital Conversion ICs

the system by setting the scale constant of the ADC. It is not considered as part of the error budget.

3. Input bias current of 2 nA (max) causes an offset error voltage in the source resistance.

Source resistance = 10 ohms (source) + 300 ohms (MPX switch)

Offset error =  $2 \text{ nA} \times 300 \text{ ohms} = 600 \text{ nV} = 0.6 \mu\text{V}$  (0.06 ppm, negligible)

4. Offset vs. temperature =  $3 \text{ mV}/110^\circ\text{C} = 27.3 \mu\text{V}/^\circ\text{C}$

Since the temperature of the chip may change by as much as  $28^\circ\text{C}$ , the total change over the range will be

$27.3 \mu\text{V} \times 28^\circ\text{C} = 756 \mu\text{V}$ , or . . . . . 75.6 ppm  
of  $\pm 10 \text{ V}$ . An offset adjustment is provided for initial trimming.

Resolution	Family	Output	Digital Input	Reference	Multiply Capability	Comments
8 Bits	AD558	Voltage	8-bit latched	Internal	1-quadrant	Single supply CMOS
	AD7224	Voltage	8-bit latched Double-buffered	External	1-quadrant	
	AD7226	Voltage	8-bit latched	External	1-quadrant	4-channel CMOS
	AD7524	Current	8-bit latched	External	4-quadrant	CMOS
	AD7528	Current	8-bit latched	External	4-quadrant	Dual CMOS
9 Bits	AD7523	Current	8-bit direct	External	4-quadrant	CMOS
		Current	9-bit latched	External	2-quadrant	LOGDAC™ CMOS
10 Bits	AD7115	Current	9-bit latched	External	2-quadrant	CMOS
10 Bits	AD7533	Current	10-bit direct	External	4-quadrant	CMOS
12 Bits	AD7542	Current	4-4-4 latched Double-buffered	External	4-quadrant	CMOS
	AD7545	Current	12-bit latched	External	4-quadrant	CMOS
	AD7548	Current	8-4 or 4-8 latched Double-buffered	External	4-quadrant	CMOS
	AD7549	Current	4-4-4 latched Double-buffered	External	4-quadrant	2-channel CMOS
	AD7541	Current	12-bit direct	External	4-quadrant	CMOS
	AD567	Current	4-4-4 latched Double-buffered	Internal	2-quadrant	CMOS
	AD667	Voltage	4-4-4 latched Double-buffered	Internal	2-quadrant	4-channel Hybrid
	AD390	Voltage	12-bit latched Double-buffered	Internal		
	AD565A	Current	12-bit direct	Internal	2-quadrant	
	AD566A	Current	12-bit direct	External	2-quadrant	
14 Bits	AD DAC80	Optional	12-bit direct	Internal	2-quadrant	CMOS
	AD7240	Voltage	12-bit direct	External	1-quadrant	
	AD7534	Current	6-8 latched Double buffered	External	4-quadrant	
	AD7535	Current	14 or 6-8 latched Double buffered	External	4-quadrant	
16 Bits	AD569	Voltage	8-8 latched Double-buffered	External	2-quadrant	Hybrid CMOS
	ADDAC71/72	Optional	16-bit direct	Internal	2-quadrant	
	AD7546	Voltage	16-bit latched	External	2-quadrant	

Table 11.2 General-Purpose Digital-to-Analog Conversion ICs

5. Offset vs. power supply is equal to  $-70 \text{ dB}$ , or  $0.316 \times 10^{-3} \text{ V/V}$ .

Since the supply may vary by  $150 \text{ mV}$ , or  $1\%$  of  $15 \text{ V}$ , the error contribution is  $47.4 \mu\text{V}$ , or . . . . . **4.7 ppm**

By an analysis comparable to the above, we would normally also prepare a system timing diagram, and assign operate-and settling-time allowances. However, the components selected for this example have more than adequate settling time, even for  $0.01\%$  operation; consequently, we can overlook the need for a formal timing analysis to determine whether settling times are adequate.

### *Converter*

1. Specified linearity error (relative accuracy) of AD574AL:  $\frac{1}{2} \text{ LSB}$ , or . . . . . **122 ppm**

2. Quantizing uncertainty:  $\frac{1}{2} \text{ LSB}$ , or  $0.0125\%$ . This is a resolution limitation, not normally considered in the error budget.

3. Temperature errors

a. Gain temperature coefficient:  $10 \text{ ppm}/^\circ\text{C}$  for  $30^\circ\text{C}$

$10 \text{ ppm}/^\circ\text{C} \times 30^\circ\text{C} = 0.03\%$ , or . . . . . **300 ppm**

b. Zero temperature coefficient:  $10 \text{ ppm}/^\circ\text{C}$  for  $30^\circ\text{C}$

$10 \text{ ppm}/^\circ\text{C} \times 30^\circ\text{C} = 0.03\%$ , or . . . . . **300 ppm**

4. Power supply sensitivity error:  $2 \frac{1}{2} \text{ LSB}$  for worst-case  $10\%$  change in all three supplies. For a  $1\%$  shift, the error is  $0.25 \text{ LSB} = 0.000061$ , or . . . . . **61 ppm**

5. Differential nonlinearity temperature coefficient: guaranteed 12-bit resolution with no missing codes over temperature.

In this example, the worst-case arithmetic sum of these errors is  $0.096\%$ , and the rms sum is  $0.046\%$ . Because they are based on conservative assumptions, these error levels in the conversion stage are consistent with a specified error of  $0.1\%$ . The designer can go on to the other hardware, software, interface, and wiring problems.

## CONCLUSION

In this chapter, we have sought to make the designer's process of choosing a converter easier and more effective by providing checklists of relevant questions in making a choice, definitions of specifications and related features, converter charts, and an example of selection and evaluation. We now go on to some considerations for what must be done to make the system work as expected.



# Chapter Twelve

## Applying Converters Successfully

In Chapter 11, we pointed out that selecting the most economical converter for an application is not a simple task, considering the many different types of converters on the market, the complex manner in which converter specifications relate to a specific system application, and the fact that prices of converters range from less than \$10 to several hundreds of dollars.

In this chapter, we will discuss system aspects of selecting converters, a continuation of the discussion in the last chapter.

To make the most appropriate converter choice requires that the user consider a number of questions: What are the real objectives of the conversion process, and how do they relate to the converter's specifications? How may the system be configured to relax the converter's performance (and price) requirements, and at what overall cost? How will the other system components limit and degrade the converter's performance? What tradeoffs are available in the system error budget? Is it more economical to make a long-term choice of one "general-purpose" converter, which will meet the needs of a large number of system designs with a single standard configuration, or to go through an optimum selection process for each individual application?

After selecting the appropriate converter, the user should be fully aware that the thorough preliminary analysis and economic component choice usually involved are not by themselves sufficient to ensure that the system performance needs will be met. The system designer must take into account the physical surroundings, interconnections, grounding and power supplies, protection circuitry, and all the other details that constitute good engineering practice.

While these few pages cannot (and are not intended to) be a primer on engineering practice, it is essential for the converter user to become aware of

those elements of practice that are of particular relevance to converter-system design.<sup>1</sup>

## 12.1 MAKING THE PROPER SYSTEM CHOICES

A general rule of thumb used by some designers may be expressed as follows: "As the converter performance requirements approach state-of-the-art converter capabilities in *both speed and accuracy*, the price of the converter will increase exponentially." If substantial cost savings are desired, the user must relax one of these parameters.

### 12.1.1 DATA-ACQUISITION SYSTEMS

An example will serve to illustrate the process of elimination and winnowing that can be profitably employed to determine a converter's minimum performance requirements. Figure 12.1 shows, in the simplest terms, a block diagram of an analog data-acquisition system, the primary application for which A/D converters are used.

The data-acquisition system, under the direction of the control unit, selects the multiplexer input points, one at a time, and directs the signal appearing on each point to the analog input of the A/D converter via the associated multiplex channel. The signal level is encoded by the converter and outputted to storage. The storage unit retains each piece of data in a predetermined format, and holds it for further processing.

### 12.1.2 THREE CLASSES OF CONVERTER SPECIFICATIONS

In attacking the problem of determining the converter performance requirements, it is useful to divide the converter specifications into three classes: Those that determine accuracy under optimum conditions, those that are dependent on time (or speed of response), and those that are substantially affected by the environment.

In the first class are included resolution, relative accuracy, differential linearity, noise, quantization uncertainty, monotonicity, and differential-linearity

<sup>1</sup>Useful (and strongly recommended) references include:

1. *Analog Devices 1984 Databook* (or subsequent editions). Integrated Circuits, Vol. I. (Norwood: Analog Devices, Inc.) Application Notes:

"An I.C. Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," pp. 20-13 to 20-20.

"Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs," pp. 20-37 to 20-40.

"Shielding and Guarding," pp. 20-85 to 20-90

"Understanding Interference-Type Noise," pp. 20-81 to 20-84.

2. Brokaw, A. Paul, "Analog Signal-Handling for High Speed and Accuracy," *Analog Dialogue* 11-2 (1977), pp. 10-16.

3. Burton, Phil, *CMOS DAC Application Guide*. (Norwood: Analog Devices, Inc.), 1984.

4. Morrison, Ralph. *Grounding and Shielding Techniques in Instrumentation* Second Edition. (New York: John Wiley & Sons, 1977).

5. Ott, Henry W. *Noise Reduction Technique in Electronic Systems*. (New York: John Wiley & Sons, 1976).

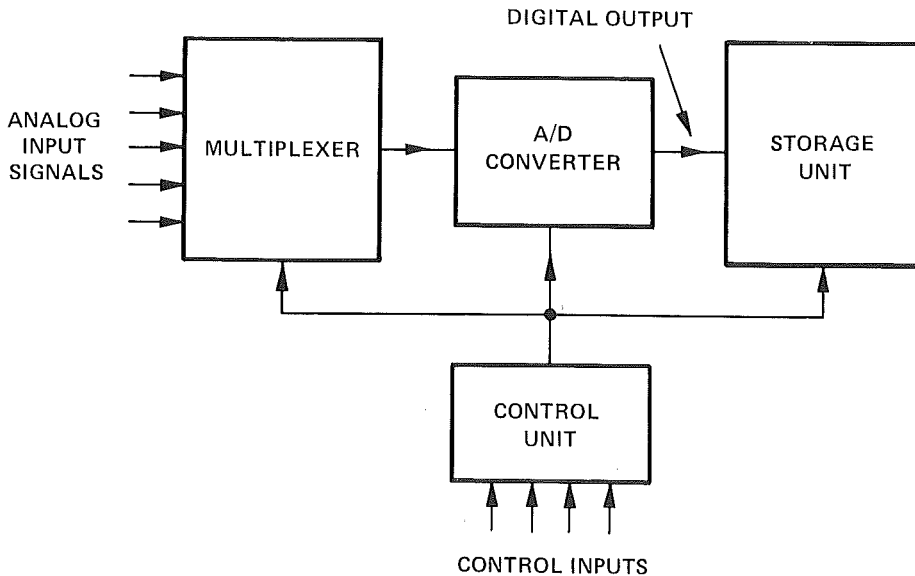


Figure 12.1. Data-acquisition system.

temperature coefficient. The reason this last term is included, though it would appear to be an environmental specification, may be somewhat unexpected: Although the ambient temperature may be in the steady state, it can be elevated (e.g., 25°C above normal room temperature) by virtue of enclosure in a cabinet. Although calibration *in situ* can correct for errors produced by variation of gain and offset with temperature, no correction can normally be effected for errors characterized by the differential-linearity T.C., due to individual bit variations with temperature. For this reason, the differential-linearity error at 25°C is augmented by the product of the steady-state temperature rise and the differential-nonlinearity temperature coefficient.

Speed-dependent specifications, in the second category, include conversion time, bandwidth, settling time of the input circuitry, etc. Environment-related specifications in the third category include gain (i.e., scale-factor) tempco, offset tempco, limits of the operating temperature range, etc.

### 12.1.3 APPROACHES TO RELAXING THE SPECIFICATIONS

Relaxation of the specifications in the first class may be effected through the use of signal conditioners. Choice of the specific form signal conditioning may take is based on our knowledge of the input signals to be encoded and the information to be extracted from the encoded data. Known or unwanted signal components may be removed from the input signals, and the peak-to-peak variation of the remaining signals may be scaled to equal the input voltage range of the a/d converter, using an analog subtractor having adjustable gain.

For example, if the signal conditioner is a differential instrumentation amplifier, such as the Analog Devices AD524 or AD624, it may be used to bias out dc offsets, and to scale the input appropriately (Figure 12.2).

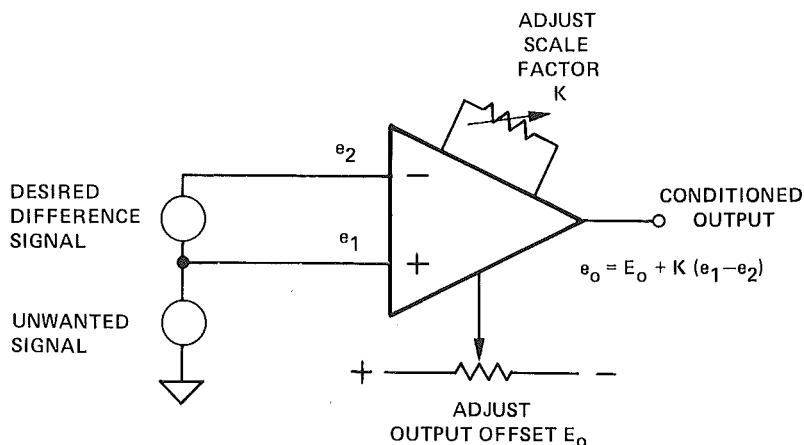


Figure 12.2. Differential instrumentation amplifier as a signal-conditioner for data acquisition.

The level-shifting-and-scaling operation can be used to obtain efficient use of the converter's input range. Scaling may allow voltage increments in the original signals, that were less than 1 LSB of the converter's input voltage range, to be measured.

#### 12.1.4 LOGARITHMIC COMPRESSION

In applications calling for wide dynamic signal range but capable of tolerating constant fractional error (e.g., 1% of actual value), rather dramatic efficiency can be realized through the use of logarithmic amplifiers for data compression, as shown in Figure 12.3.

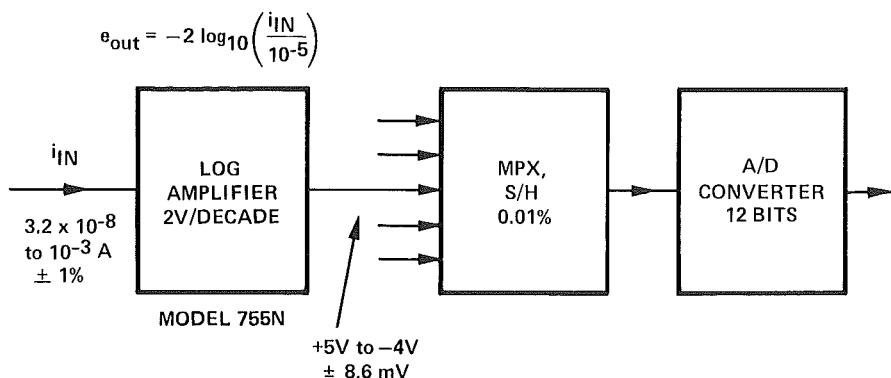


Figure 12.3. Using a log amplifier for range compression in a data-acquisition system.

Here, a logarithmic amplifier allows encoding of signals, that would ordinarily require a minimum of 20-bit conversion to handle the dynamic range, with a far-less-costly 12-bit converter. Modest accuracy in a fixed ratio to (e.g., % of) actual value is substituted for extreme accuracy in relation to the entire full-scale range, at considerably less cost. For many applications, this is an ideal performance mode; an exception is the set of applications for which extremely small errors are required at all points in the range (e.g., measuring long-term stability of voltage sources).

The logarithmic data can be dealt with easily if the data is to be processed digitally; or it can be recovered in linear analog form (if it is simply to be stored or transmitted digitally) by the use of another log amplifier, in the antilog connection, with a D/A converter; or in some cases it can be recovered by a LOG-DAC<sup>TM</sup> with appropriate connections.

### 12.1.5 FILTERING

Another commonly used signal-conditioning unit is the filter. Low-pass filters are used to extract carrier, signal, and noise components, above the frequencies of interest, from the input signals. These components appear as aliased low-frequency noise if they are above one-half the sampling frequency. A/D converters often incorporate (or require) follower circuits for impedance buffering. With a modicum of external wiring, they can be connected as active low-pass filters (Figure 12.4).

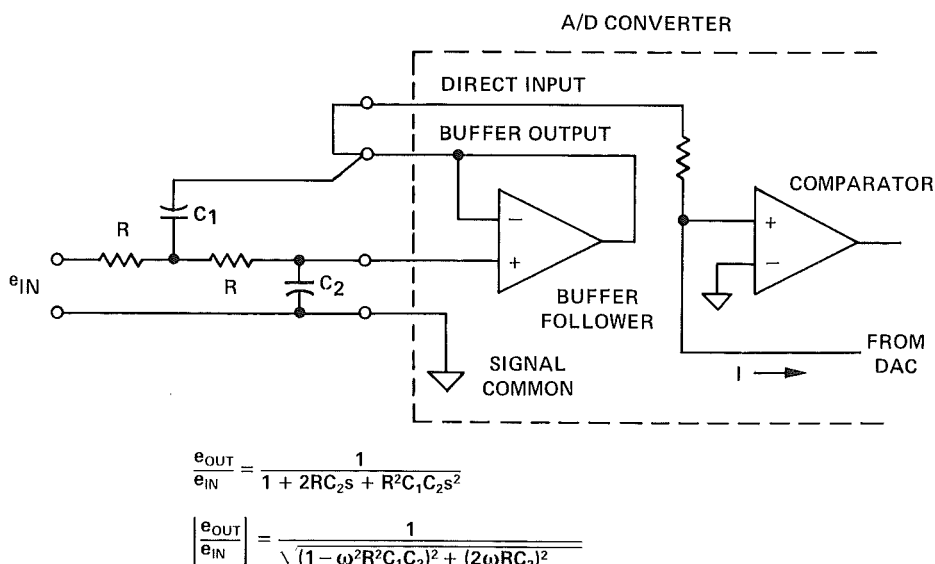


Figure 12.4. Input buffer of an a/d converter connected as an active low-pass filter.

### 12.1.6 SAMPLE-HOLD

A relaxation of the second class of specifications can also be effected by adding a sample-and-hold amplifier to the system configuration, as depicted in Figure 12.5.

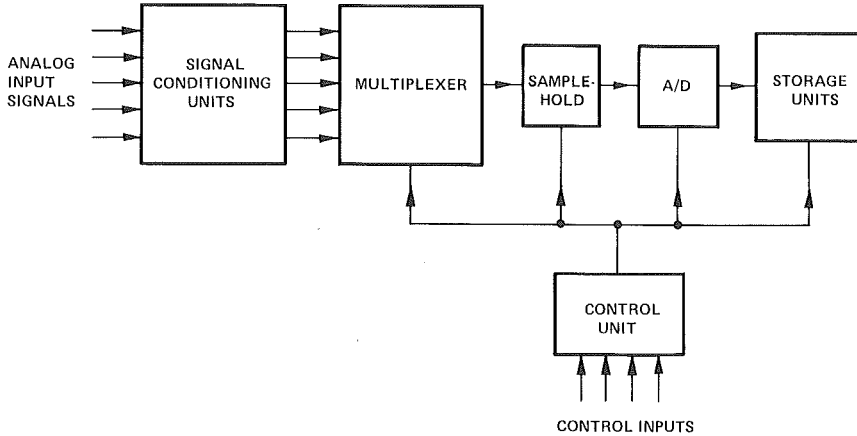


Figure 12.5. Data-acquisition system with sample-and-hold and input pre-conditioning.

The use of a sample-and-hold amplifier can substantially increase the highest signal frequency, of a given amplitude, that may be encoded within the resolution of the converter, as well as increasing the system throughput rate.

There are two sources of limitation on the maximum analog frequency that can be handled. One is the Nyquist criterion (the highest component of frequency in the analog signal cannot exceed one-half the sampling frequency); this limits analog signals to one-half the throughput rate. The other has to do with the timing of the sample. The following example shows what the problem is and indicates the improvement possible with a sample-and-hold: If the input is a sine wave,  $E_p \sin(2\pi f t)$ , with  $E_p = \text{F.S.}$ , the maximum rate of change occurs at zero and, as can be found by differentiating with respect to  $t$ , is equal to  $2\pi f E_p$ . If the change in the input to the converter is to be less than 1 LSB during the conversion, then

$$\text{Max. Rate} = 2\pi f E_p = \frac{1 \text{ LSB}}{\Delta t} = \frac{2^{-n} \cdot 2 E_p}{\Delta t} \quad (12.1)$$

and the highest frequency that can be applied is

$$f_{\text{MAX}} = \frac{2^{-n}}{\pi \Delta t} \quad (12.2)$$

where  $2 E_p$  is the peak-to-peak signal span, and  $\Delta t$  is the time uncertainty as to when the conversion took place (equal to the conversion time for successive-approximation converters). For a 12-bit converter with a 20- $\mu\text{s}$  conversion time,  $f_{\text{max}}$  is about 4Hz! Using a sample-and-hold, one can reduce the uncer-

tainty in the time of measurement from the ADC's conversion time to the aperture-time uncertainty of the sample-hold, thus effecting a possible improvement in  $f_{\max}$  by the ratio of the conversion time to the aperture-time uncertainty.

Since aperture jitter of the order of nanoseconds is routinely available in sample-holds designed for operation with 12-bit converters (the AD585 has an aperture-jitter specification of 0.5 ns), an improvement greater than 10,000:1 is quite feasible, assuming that the S/H has adequate bandwidth. Thus, the limitation of 4 Hz would become 40 kHz; but at a sampling rate of 50 kHz  $1/(20\mu\text{s})$ , the highest signal component would be limited to 25 kHz by the Nyquist criterion. The sample-hold's phase shift for 20-kHz signals is only  $0.6^\circ$ . Thus, this sample-hold application would be quite conservative with regard to timing.

The sample-hold can also increase the system throughput rate. The system throughput rate, without the sample-hold, is determined primarily by the multiplexer's settling time, plus the A/D converter's conversion time.

The multiplexer settling time is the time required for an analog signal to settle to within its share of the system error budget, as measured at the input to the converter, after selection by the multiplexer. For a 12-bit conversion system, with a  $\pm 10\text{V}$  range, multiplexers typically settle within 1 microsecond, and typical conversion times are 20 microseconds. The sample-hold can be used to hold the last channel's signal level for conversion, while the next channel is selected and settles. Since sample-hold amplifiers with acquisition times of less than  $5\mu\text{s}$  to within 0.01% are readily available (for example, the AD585 has a maximum acquisition time of 3  $\mu\text{s}$  to 0.01% for 10-volt changes), the throughput period can be reduced to approach the conversion time. Pairs of sample-holds and A/D converters can be used for alternate conversions to increase throughput rate even further, though at somewhat higher cost.

If the speed of a/d conversion is significantly limited by the settling time of an ADC's input buffer-follower, the sample-hold may be connected to bypass it, providing an even greater increase in throughput rate.

Relaxation of the third class of errors, those due to environment-related specifications, may be abetted by allotting one multiplexer channel to carry a ground-level signal, and another to carry a precision reference-voltage level that is near-full scale. Data obtained from these channels may be used by a processor to correct gain and offset variations common to all channels, generated in the sample-hold, the A/D converter, and the associated wiring.

### 12.1.7 DRIVING THE ANALOG-TO-DIGITAL CONVERTER

Since the sample-hold is used to create an effectively "dc" input signal during the conversion interval, a sample-hold will be unnecessary if the signal is already varying slowly enough to be, in effect, a dc signal.

However, there may be a trap! Many designers overlook the fact that, besides holding the input signal constant during the conversion, the sample-hold amplifier also has a quite low output impedance (in most cases), which is a requirement for driving the analog input of many a/d converters.

To understand the need for low dynamic output impedance, consider this: for a 12-bit converter, such as the AD574A, with a conversion time of  $25\text{ }\mu\text{s}$ , the clock rate of the successive-approximation register is about  $(12\text{ comparisons})/(25\text{ }\mu\text{s}) = 480\text{ kHz}$ . At each trial, the programmed current output from the d/a converter flows through the input resistor, developing a voltage drop, in opposite sense to the analog input voltage. The net voltage is sensed by the comparator, which then makes its decision (Figure 12.6a).

Since this set of 480-kHz current pulses has to flow through the output circuit of the device that furnishes the input signal, it will cause transient changes in the input (glitches)—unless the analog input is driven by an ideal voltage source having zero dynamic impedance; if these transients are sufficiently large or long-lasting, they may lead to erroneous conversions and missed codes.

Ideal voltage sources do not exist, but as long as the impedance is sufficiently low at the switching frequency of the successive-approximations register (480 kHz, in this example), the a/d converter should be able to convert accurately without encountering this kind of dynamic errors.

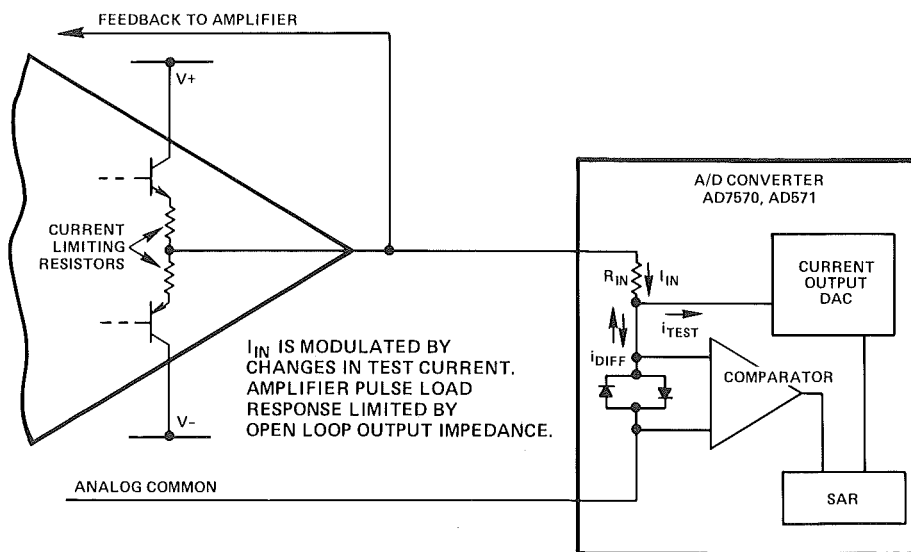
The way to get an amplifier with low output impedance is to configure a wideband high-slew-rate amplifier as a voltage follower. The closed-loop output impedance of an op amp is equal to the open-loop output impedance (usually a few hundred ohms) divided by the loop gain *at the frequency of interest*.

It is often assumed that the loop gain of a voltage follower is sufficiently high to reduce the closed-loop output impedance to a negligibly small value, especially if the signal is at low frequency. However, the amplifier driving the ADC must have either sufficient loop gain at 480 kHz to reduce the closed-loop output impedance to a low value, low open-loop output impedance, or both.

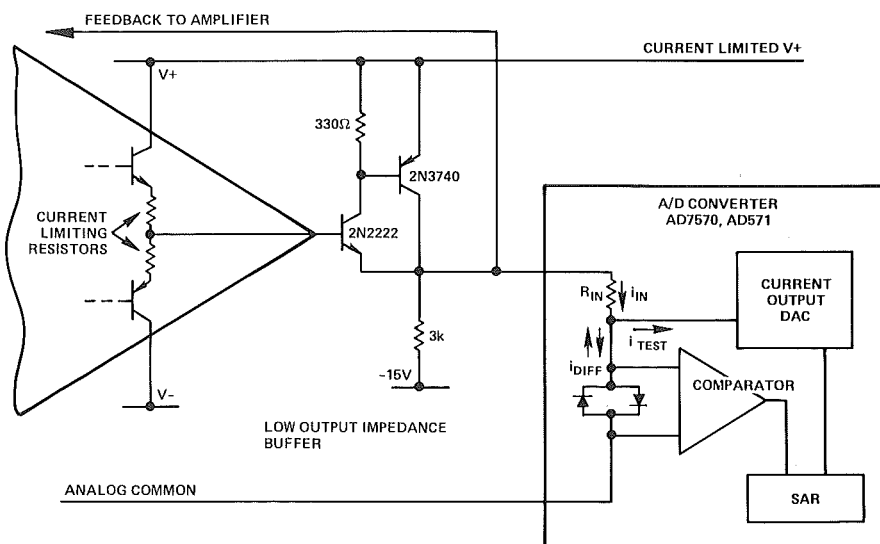
This can be accomplished either by using a wideband op amp (or sample-hold), or by connecting a discrete-transistor or integrated buffer inside the amplifier's feedback loop (Figure 12.6b) The voltage follower's output should be physically within one or two centimeters of the a/d converter; this minimizes inductance—and the problems that inductive reactance introduces.

Finally, when the system is laid out, unshielded analog signal lines should never run in channels with either digital signal lines or power lines. In applications employing printed-circuit boards, where possible, analog leads should be guarded by paralleled common leads and ground planes on the reverse side.





a. Relationship between successive-approximation a/d converter and the op amp that is the source of the input signal.



b. Inside-the-loop buffer provides stiff drive for unipolar ADC.

Figure 12.6. Driving a/d converters.

### 12.1.8 CONTRIBUTIONS TO ERROR

The decision to seek means of relaxing the required specifications is based on the availability and cost of devices that meet the original specifications, as compared to the cost of alternatives and any additional problems engendered

by departing from a straightforward approach. To evaluate the performance tradeoffs, an error budget is a useful tool.

Three classes of errors should be considered:

- Errors due to the non-ideal nature of each component
- Errors due to the physical interconnections of the system components
- Errors due to the interaction of system components.

The first group of errors can be determined from the spec sheets for the system components. The second group result from parasitic interactions that are a function of the way the interconnections are managed, e.g., grounding, shielding, contact resistance, etc. The third group result from specific interactions between components in the system; though they are not specifically called out in spec sheets, they can be predicted from careful reading of the specifications of the individual devices, or from the user's knowledge of how they are designed.

An example of this class of error sources might be the offsets created by series impedances in the signal path (signal-source impedance, multiplexer-switch *on* impedance) and the bias and leakage currents of the stages following these impedances, to which they are connected. A second example might be disturbances caused at the signal source as the multiplexer switches it into the circuit.

By showing where the important contributions to error are, the error budget is used as a tool for establishing tradeoffs to set the final performance requirements for the system. The error budget can be used as a tool in predicting the overall expected error, whether by worst-case summation, by root-sum-of-the-squares summation, or by combinations of the above using specific knowledge of possible compensations and common sense.

## 12.2 INSTALLATION AND GROUNDING

The current popularity of modular converters, in the form of modules, hybrids, and ICs, makes it worthwhile to consider some elements of their design.

For one thing, many types are "customer-programmable." This means that the user may select one of several possible signal voltage ranges by choosing the appropriate jumper-wiring configuration at the device's terminals. It goes without saying that all terminals used to determine the signal voltage range involve analog signals; to protect their low resolution levels, they should be kept away from circuit-card etch runs that carry logic signals.

User-programmable inputs, in addition to their jumpering possibilities, also permit modification by the connection of external resistors. Care should be exercised in doing this, for the reasons mentioned above. In addition, it should be noted that the excellent gain and offset T.C.'s of these devices are achieved by depending, not on absolute stability with temperature, but rather on the close tracking with temperature of key resistors within the device.

Therefore, even if 0 ppm/°C TCR resistors are used externally, the overall gain and offset performance vs. temperature may be appreciably degraded. Since there may be ways of avoiding excessive errors, the manufacturer should be consulted before external resistors are “frozen” into the design.

In the design of the converter module, great care is taken to separate the analog and digital signal lines. This procedure should also be followed with the external layout of the board on which the converter is mounted. Etch runs of digital signal lines should not run parallel in close proximity with etch runs of analog signal lines. If these lines must cross, they should do so at right angles.

Particular care should be taken with sensitive low-level points, e.g., the comparator input on a/d converters and the summing junction of the output amplifier on d/a converters. Etch runs to these points should be as short as possible. Analog-ground guard runs may also help reduce interference.

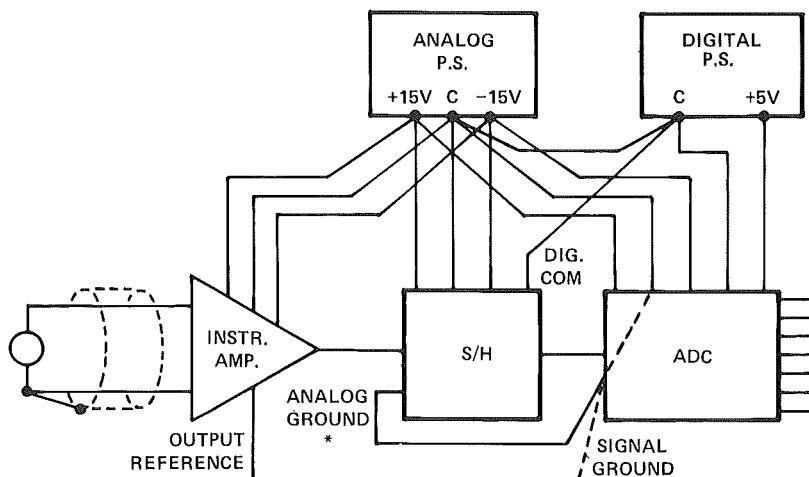
### 12.2.1 GROUNDING

Converter modules (actually, most data-acquisition components) have a number of ground terminals, which are generally not connected together within the module. These “grounds” are usually referred to as Digital Common, Analog Common (Analog Power Return), and Analog Signal Ground (or Sense). These grounds must be tied together at one point, the system star point, or “Mecca,” usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts could be generated between the system star point and the ground terminal of the module. Separate ground returns are provided to minimize the current flow in the path from sensitive points to the system star point. In this way, supply currents do not flow in the same return path with analog signals, and logic-gate return currents are not summed into the return from a precision reference-zener diode. (Figure 12.7)

In any event, the connections between the system star point and the ground terminals should be as short as possible and should have the lowest feasible impedance.

Each of the device’s supply terminals should be capacitively decoupled to the appropriate ground point (see Section 12.4.2), as close to the device as possible. A large-value capacitor with a high resonant frequency should be used. A 15  $\mu$ F solid-tantalum capacitor is usually sufficient. Analog supply terminals are bypassed to the appropriate power return terminal, and the logic-supply terminal is bypassed to the logic power return terminal.

When gain and offset adjustments are available and are intended to be used, the potentiometers for performing the adjustments should be mounted (with



\*IF INDEPENDENT. OTHERWISE, RETURN AMPLIFIER REFERENCE TO MECCA AT ANALOG P.S. COMMON

Figure 12.7. A popular (but by no means universal) approach to grounding. Grounding practice must be individually tailored to the structure of a particular system and the characteristics of the components employed, taking into account where the various signal and foreign currents actually appear at the device terminals.

short leads) in such a position that they will be accessible when the mounting board is installed in the system.

The same care should be taken to locate a conversion subsystem properly within a system as is taken to mount a conversion device on its circuit board. A converter should never be located near a transformer or fan blower motor. Using mu-metal shielding to protect against electromagnetic and RFI pickup is an expensive and not-always-successful proposition.

D/A converters should be located at their loads. This may require long cable runs for the digital control signals; however, the reduction in noise pickup and ground-potential differences between the D/A's output and the load can easily justify the expense. An alternative where this is simply not possible, as in component testing, is to use force-sense connections, in which the voltage at the load is sensed, compared with the desired value, and feedback circuitry applies whatever forcing voltage is required to minimize the error (see Figure 6.3).

For more on grounding and bypassing, see Section 12.4.2.

### 12.2.2 REDUCING COMMON-MODE ERRORS

As we have indicated, a differential amplifier may be used to eliminate the effects of ground-potential differences in various parts of the system in which the converter is used. In Figure 12.8, the signal source is a remotely located transducer, and the differential amplifier is located near the A/D converter.

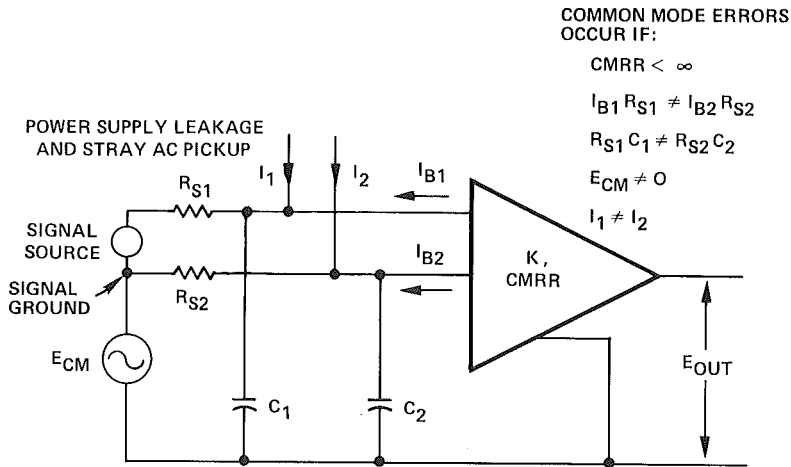


Figure 12.8. Common mode and the difference signals due to line unbalance.

The common-mode signal is the potential difference between the ground signal at the converter and the ground signal at the transducer, plus any undesirable common-mode signal produced by the transducer, and any voltages developed across the unbalanced impedances of the two lines.

If the signal source is the output of the system's d/a converter, the differential amplifier would be located near the remote load. The common-mode signal is developed by the differences in ground potential at the two locations.

The amount of dc common-mode offset that is rejected depends on the dc common-mode rejection (CMR) of the amplifier. However, bias currents flowing through the signal source leads can cause offsets, if either the bias currents or the source impedances are unbalanced. DC CMR specifications generally include a specified amount of source unbalance (e.g., 1 k $\Omega$ ). Such specifications also indicate a top frequency for which the dc spec is valid, usually the line frequency (50-60 Hz), but sometimes 100 Hz. At higher frequencies, unbalanced RC time constants (balanced or unbalanced series resistance and shunt capacitance to common, plus the amplifier's internal unbalances) reduce the common-mode rejection, by producing a normal-mode signal. This source of error can be greatly reduced by proper use of a guard shield, as shown in Figure 12.9.

Here, no part of the common-mode signal appears across the capacitors  $C_A$  and  $C_B$ , since the shield is driven by the source of the common-mode signal. The shield also provides electrostatic shielding to minimize coupling to other signal lines in close proximity to the input leads.

When installing a guard shield, it is important that the guard shield connect only at one point, to the source of the common-mode signal, and that the shield be continuous, i.e., through multiplexers, connectors, patch panels, etc. Since the shield is carrying a common-mode signal, it should be properly

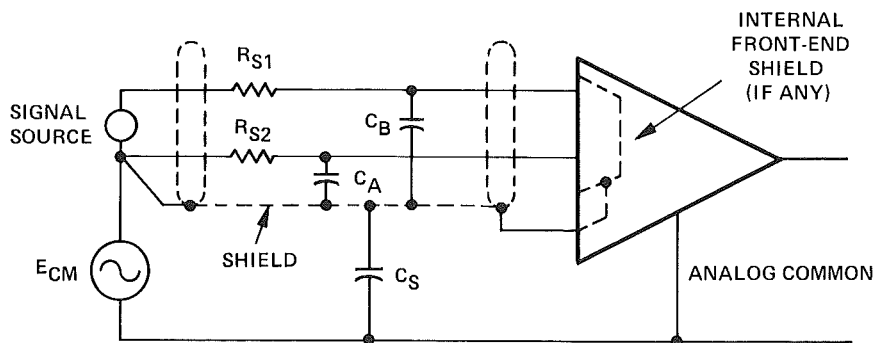
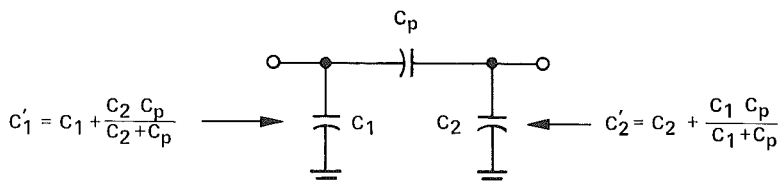
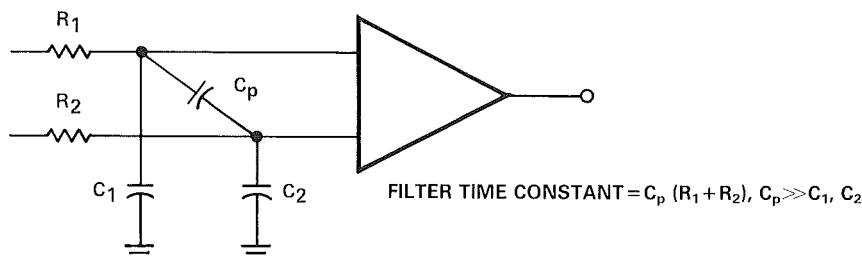


Figure 12.9. Use of guard shield to improve common-mode rejection at higher frequencies.

insulated to prevent it from shorting to other shields or the earth ground. A final precaution that should be taken is to make sure that a conductive return path exists for the bias and leakage currents of the differential amplifier (unless it is a true isolator with transformer- or optically isolated, floating inputs).

It is helpful, in reducing noise and improving common-mode rejection, to connect the largest tolerable capacitance *between* the input leads. It will provide some filtering, and will reduce the capacitive unbalance by more than its ratio to the stray capacitance. (Figure 12.10)



$$\text{If } C_1 = 1 \text{ pF}, C_2 = 2 \text{ pF}, C_p = 0.001 \mu\text{F}$$

$$C'_1 = 1 + \frac{2000}{1001}$$

$$= 1 + 1.9995 = 2.9995$$

$$\cong C_1 + C_2$$

$$C'_2 = 2 + \frac{1000}{1001}$$

$$= 2 + 0.999 = 2.999$$

$$\cong C_2 + C_1$$

Figure 12.10. Capacitance between the input leads to reduce unbalance and provide filtering.

In portions of a system where differential amplifiers are not used, i.e., where signals are all treated as single-ended signals having a common ground, sufficient precautions should be taken to insure that significant voltages are not induced in ground return leads to the single-point ground, and that the system is free from ground loops.

### 12.3 HOW TO ADJUST ZERO AND GAIN OF CONVERTERS

Many converter types are pretrimmed and require no adjustments as purchased to meet specified accuracy. However, there are cases where (1) adjustments are called for in the specifications, (2) cost-savings can be effected by trimming inexpensive pre-trimmed devices, with modest specs, for use over narrow ranges for better-than-specified accuracy, or (3) long-term corrections are necessary during years of operation. If adjustments are desired or required, for any of the above reasons, these general principles and guidelines may be helpful. Naturally, the user should follow the specific instructions published in product data sheets, especially where there are conflicts.

Proper adjustment of zero and gain in DACs and ADCs is a procedure that requires great care and extremely sensitive reference instruments. The voltmeter used to read the output of a DAC, or the voltage source used as a driving signal for the ADC, must be capable of stable and clear resolution of 1/10 LSB at both ends of the range of the converter; e.g., at zero and full scale.

Most DACs and successive approximation ADCs manufactured by Analog Devices are provided with Zero and Gain adjustments *which are completely independent of each other*, as long as the adjustment of Zero is attempted *only* when the input code is calling for Zero, and as long as the Zero (or Offset) adjustment is accurately completed before proceeding to adjustment of Gain (at Full Scale – 1 LSB). Of course, it is possible to make Zero and Gain adjustments in reverse order and at other points on the transfer function—but it must be expected that the adjustments will no longer be independent, and the procedure will require a series of successive approximations.

#### 12.3.1 ADJUSTMENT PROCESS

Particularly for bipolar converters, fast and successful adjustment requires knowledge of the technique used in the circuit to configure the inherently unipolar DAC or ADC for bipolar operation.

1. Sign & Magnitude Codes are generally obtained by use of a unipolar converter with separate means of reversing polarity. The Zero adjustment is always made by calling for a zero from the converter. (Logic zero into a DAC produces zero volts output, or zero volts into an ADC produces data-zero output.)

2. Bipolar binary converters utilizing offset binary or twos complement coding usually employ analog offsetting to convert a unipolar design into bipolar.

For instance, a 0 to +10V DAC may have its output amplifier offset by  $-5\text{V}$ , resulting in an output of  $-5\text{ volts}$  corresponding to  $00 \dots 0$  input and  $+5\text{ volts}$  (minus 1 LSB) corresponding to a  $11 \dots 1$  input. *Such a converter should have its "Zero" adjusted at  $-5\text{V}$  ( $100 \dots 0$  in 2's complement).*

Stated another way: with positive-true logic, converter Zero controls should always be set at the "All Bits Off" condition, and then Gain should be set at the "All Bits On" condition.

### 12.3.2 ADJUSTMENT FOR DACS

**ZERO:** set the input code so that all bits are "off", then adjust the pot until the output signal is within  $\frac{1}{10}$  LSB of proper reading, or zero.

**GAIN:** set the input code so that all bits are "on", then adjust the pot until the output signal reads within  $\frac{1}{10}$  LSB of *Full Scale less 1 LSB*.

### 12.3.3 ADJUSTMENT FOR ADCS

**ZERO:** set the input voltage precisely at  $\frac{1}{2}$  LSB above the "all bits off" specified input. The zero control should be adjusted so that the converter just switches in its LSB.

**GAIN:** set the input voltage precisely at  $\frac{1}{2}$  LSB less than "all bits on" input. Note that this is  $1\frac{1}{2}$  LSBs less than the nominal full scale value: i.e., all-1's value of a 0 to +10V 12-bit ADC is actually  $+9.9976\text{V}$ . The gain adjustment should be made with an input  $\frac{1}{2}$  LSB less, or  $+9.9963\text{ volts}$ . With the input voltage set as described, the GAIN control is rotated to the point where the last bit just comes on. For instance, in a 12 bit binary converter, a reading of 1111 1111 1110 would change to 1111 1111 1111.

It is important to note that this discussion is relevant for *offset-binary, positive-true* coding. For 2's complement, the "all-bits-off," positive-true condition is  $100 \dots 00$  and "all bits on" is  $011 \dots 11$ . For negative-true devices, the "all-bits-off" condition is  $111 \dots 11$  in offset binary,  $011 \dots 11$  in two's complement. When in doubt (or to avoid doubt), consult the data sheet.

Resolution	$\frac{1}{2}$ LSB	1 LSB	FSR $- 1\frac{1}{2}$ LSB	FSR $- 1$ LSB	FSR
8 bits	39 mV	78 mV	19.88 V	19.92 V	20.00 V
10 bits	9.8 mV	19.5 mV	19.971 V	19.980 V	20.000 V
12 bits	2.4 mV	4.88 mV	19.9927 V	19.9951 V	20.0000 V
14 bits	610 $\mu\text{V}$	1.22 mV	19.9982 V	19.9988 V	20.0000 V
16 bits	152 $\mu\text{V}$	305 $\mu\text{V}$	19.99954 V	19.99969 V	20.00000 V

Table 12.1. Checkpoints for unipolar d/a and a/d Converters with 20-V Full-Scale Range; Subtract 10 V for  $\pm 10\text{V}$  range.



Resolution	$\frac{1}{2}$ LSB	1 LSB	FSR - $1\frac{1}{2}$ LSB	FSR - 1 LSB	FSR
8 bit	19.5 mV	39 mV	9.941 V	9.961 V	10.000 V
10 bits	4.9 mV	9.8 mV	9.985 V	9.990 V	10.000 V
12 bits	1.2 mV	2.4 mV	9.9963 V	9.9976 V	10.0000 V
14 bits	305 $\mu$ V	610 $\mu$ V	9.99908 V	9.99939 V	10.00000 V
16 bits	76 $\mu$ V	153 $\mu$ V	9.999771 V	9.999847 V	10.00000 V

Table 12.2. Checkpoints for d/a and a/d Converters with 10-V Full-Scale Range (0 to 10 V); subtract 5 volts for  $\pm 5$  V.

Resolution	$\frac{1}{2}$ LSB	1 LSB	FSR - $1\frac{1}{2}$ LSB	FSR - 1 LSB	FSR
8 bits	9.8 mV	19.5 mV	4.971 V	4.980 V	5.000 V
10 bits,	2.4 mV	4.9 mV	4.9927 V	4.9951 V	5.0000 V
12 bits	610 $\mu$ V	1.2 mV	4.9982 V	4.9988 V	5.0000 V
14 bits	153 $\mu$ V	305 $\mu$ V	4.99954 V	4.99969 V	5.00000 V
16 bits	38 $\mu$ V	76 $\mu$ V	4.999885 V	4.999923 V	5.000000 V

Table 12.3. Checkpoints for d/a and a/d Converters with 5-V Full-Scale Range (0 to 5 V); subtract 2.5 V for  $\pm 2.5$  V.

## 12.4 OTHER WAYS TO IMPROVE PERFORMANCE

### 12.4.1 PRESERVING DAC ANALOG OUTPUT ACCURACY.

In all too many applications, a DAC's accuracy is subverted by the associated op-amp circuitry.

**Dynamic Problems.** The output impedance of a current-mode DAC can generally be treated as a parallel combination of resistance and capacitance. But capacitance at the output of a DAC (Figure 12.11) can produce undesirable results. The capacitance and the feedback resistance combine to add a pole to the open-loop response, resulting in reduced phase margin, which will hurt the closed-loop response.

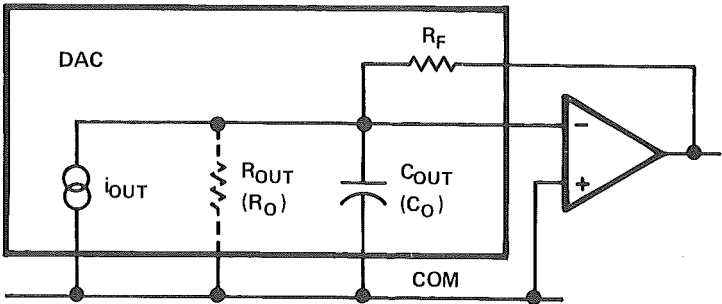


Figure 12.11. Equivalent circuit of current-output ADC.

Figure 12.12 shows how the open-loop amplitude and phase response might appear if the spurious pole due to  $C_o$  is below the crossover frequency of the undisturbed system. Not only will the closed-loop bandwidth be reduced, but—more seriously—excess phase shift will be introduced. The extra phase

shift reduces the system frequency stability margins and may cause ringing (and perhaps even oscillation).

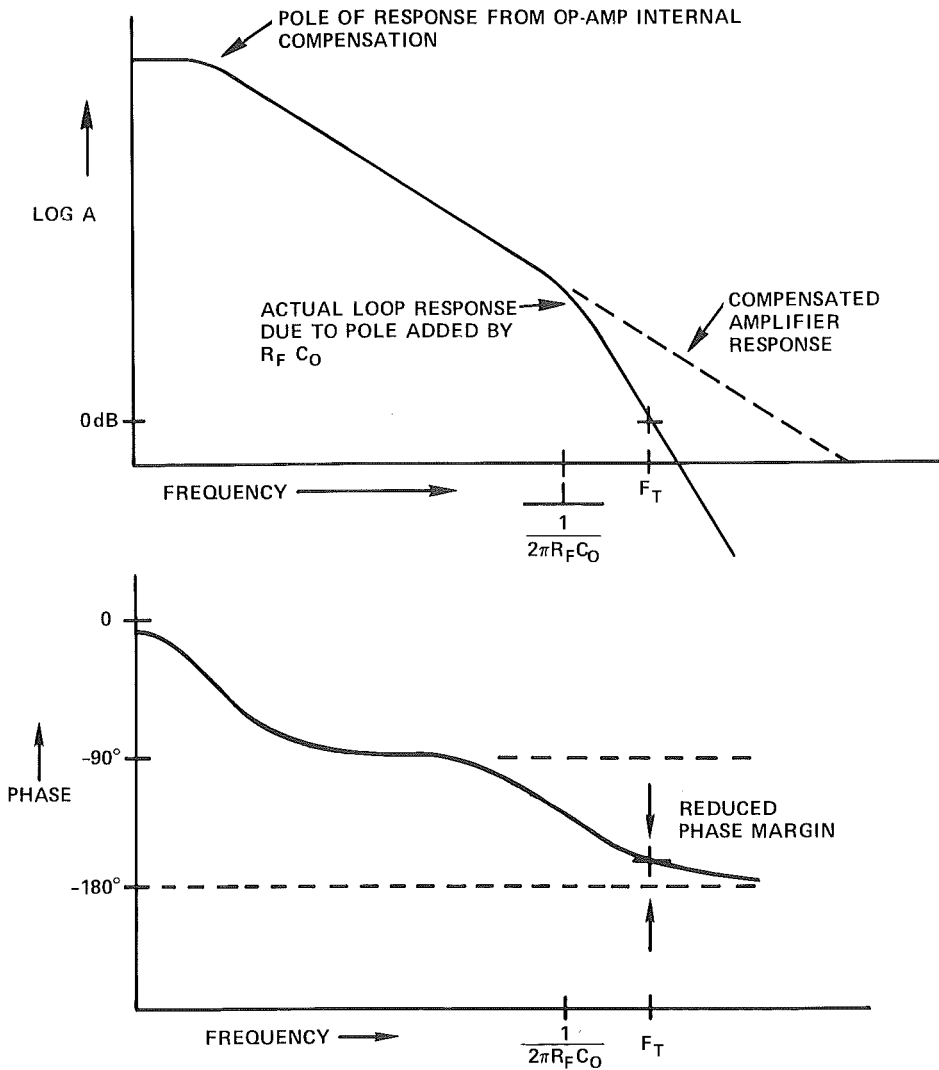
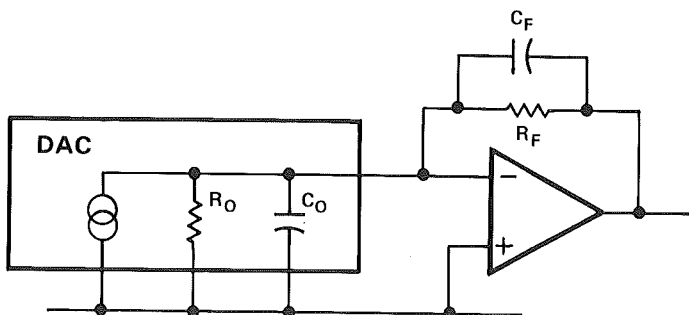


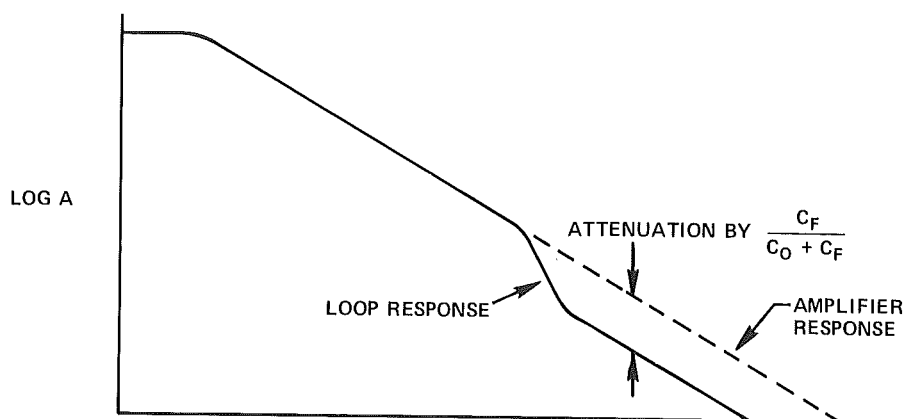
Figure 12.12. Amplitude and phase response of the circuit of Figure 12.11. The additional pole increases settling time by reducing bandwidth and increasing both overshoot and ringing.

As Figure 12.13a shows, the loop-stability margins can be restored by connecting a feedback capacitor,  $C_F$ , in parallel with the feedback resistor. This capacitance creates a zero in the open-loop transfer function, which can be adjusted to correct the phase margin. However, if  $R_o$  is quite large (as is often the case with current-output DACs), a large pole-zero mismatch may remain (Figure 12.13b).

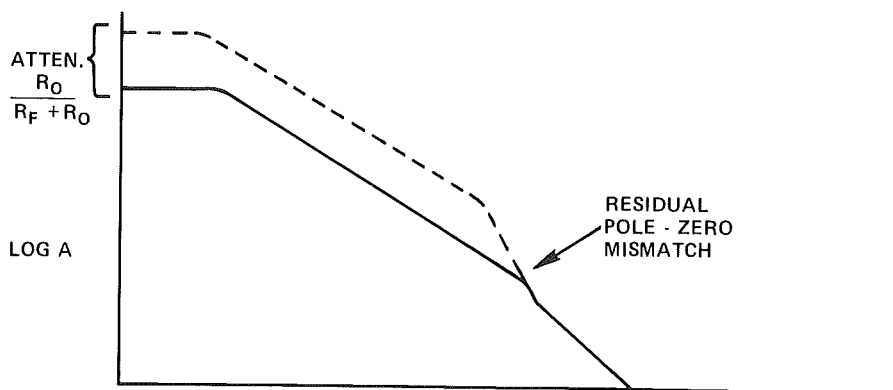
Even with finite values of  $R_o$ , a small residual pole-zero mismatch (Figure 12.13c) may result. In addition, pole-zero mismatch within the amplifier itself can lead to long-settling “tails”: the DAC output voltage may appear to settle quickly, but then it slowly changes—by a significant amount—to its final value, over the course of tens of microseconds, or even milliseconds.



a. Improving loop stability by the use of feedback capacitance,  $C_F$ .



b. Response of circuit (a), neglecting  $R_o$ . Pole-zero mismatch may yield poor transient response.

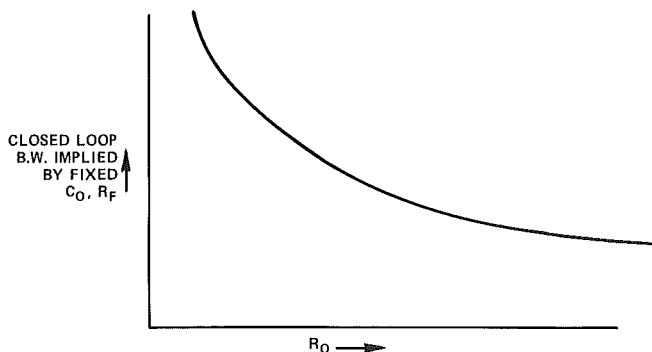


c. Response of circuit (a) with finite  $R_o$ .

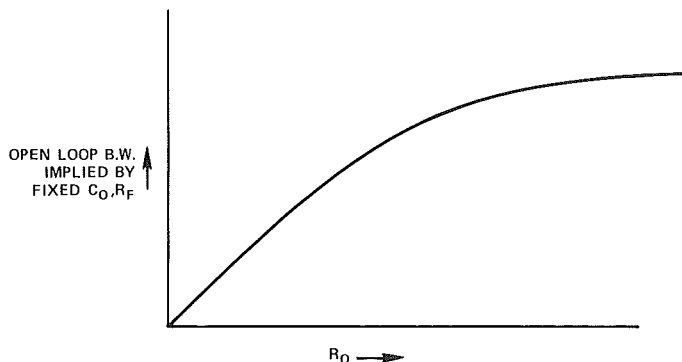
Figure 12.13. Use of feedback capacitor.

The residual external mismatch will be eliminated when the DAC's output circuit and the feedback network form a frequency-compensated voltage divider, i.e., when  $R_o C_o = R_F C_F$ . This condition can usually be satisfied, but sometimes it requires large values of  $C_F$ . Unfortunately,  $C_F$ —which is used to introduce an open-loop zero—also produces a closed-loop pole, which reduces the overall bandwidth and results in increased settling time.

$R_F$  is generally fixed by the desired DAC gain; the minimum value of  $C_o$  is a property of the converter that is not under the system designer's control. Therefore,  $C_F$  and  $R_o$  are the only two parameters that can be manipulated to improve performance (by shunting). As  $R_o'$  (the effective value of  $R_o$ ) is reduced by shunting the DAC output with a resistor, the required value of  $C_F$  is reduced, and the closed-loop bandwidth is increased (Figure 12.14a). The unity-gain bandwidth of the op amp,  $b$ , limits the open-loop system bandwidth, which—in turn—limits the realization of closed-loop bandwidth. As  $R_o'$  is reduced, the *open-loop* bandwidth obtainable for a fixed op-amp bandwidth,  $b$ , is also reduced (b).



a. Smaller values of  $R_o$  increase the closed-loop bandwidth.



b. Smaller values of  $R_o$  decrease the open-loop bandwidth.

Figure 12.14. Effect of varying  $R_o$  ( $R_o'$ ) on open-loop and closed-loop bandwidth.

An empirical compromise can be reached by adjusting  $R_o'$  to provide the same open- and closed-loop bandwidth. For a fixed  $C_o$  and  $R_F$ , the values of  $R_o'$  and  $C_F$  can be determined from

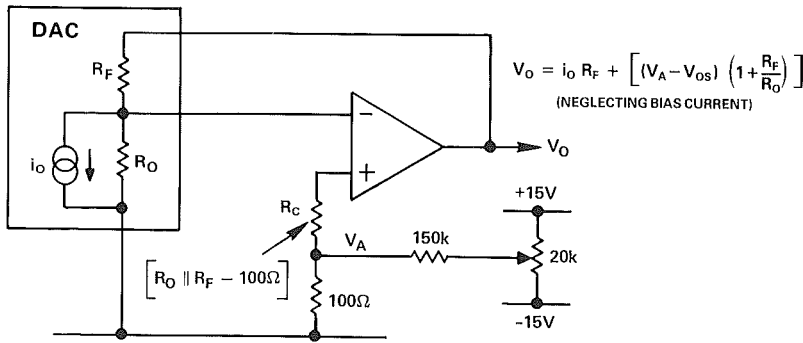
$$R_o' = \frac{1 + \sqrt{1 + 8 b \pi R_F C_o}}{4 b \pi C_o}$$

$$C_F = \frac{1 + \sqrt{1 + 8 b \pi R_F C_o}}{4 b \pi R_F} \quad (12.3)$$

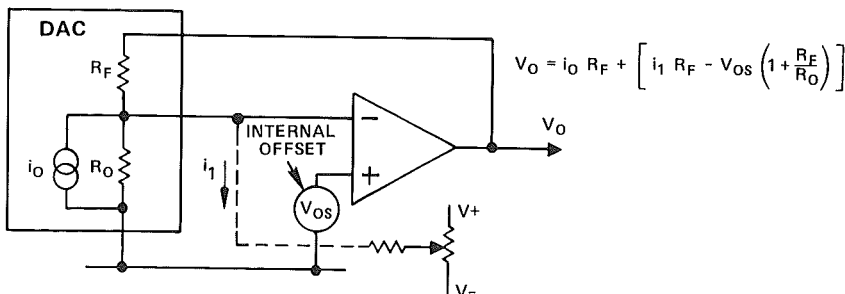
### Offset Problems in CMOS DACs.

Perhaps the best way to control  $V_{os}$  in an op amp used with a DAC is at the source—choose an op amp with sufficiently low offset and bias current over the temperature range. The next best way is to null the op-amp's offset by the manufacturer's standard recommended  $V_{os}$  trim, taking pains to connect the pot wiper to the appropriate supply terminals *at the device*.

The amplifier's offset-trim adjustment should be used *only* for  $V_{os}$  nulling; if it is used to compensate for offsets caused by the flow of bias current through the feedback resistor, as well as for offsets occurring in external circuitry, the amplifier input stage will have to be unbalanced, which will cause its  $V_{os}$  tempo to be degraded.



a. Nulling offset with voltage applied to op-amp reference input.



b. Nulling offset with current added at op-amp summing point (not recommended).

Figure 12.15. External offset-null methods.

If the amplifier lacks offset terminals, there are two commonly used ways of providing the trim; they are shown in Figure 12.15. The more-desirable approach is shown in (a); the correction is applied to the amplifier's positive input terminal, as a voltage. Since it is effectively in series with  $V_{os}$ , the  $V_{os}$  correction is unaffected by changes of  $R_o'$ ; if the amplifier has low bias current, the output offset will be independent of changes of  $R_o'$ .

The less-effective way (popular, but not recommended) is to introduce a current at the summing point, as shown in (b). If the resistances in the circuit (including  $R_o$ ) are constant, there is no problem. However, if  $R_o'$  can vary, the output offset will change, even if bias current is negligible. If the change of  $R_o'$  is a function of the applied *digital code*, the result can be increased differential nonlinearity.

For example, if the DAC is an inverted R-2R-ladder type, as shown in Figure 12.16, the output resistance,  $R_o$ , is a function of the number of switches that are closed. If all switches are open,  $R_o$  is infinite; if all (or many) switches are closed,  $R_o$  will approach  $R$ ; and if only a single switch is closed,  $R_o$  will be about  $3R$ .

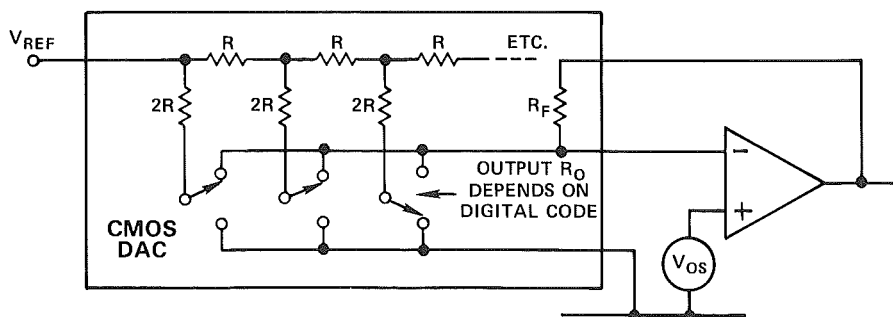


Figure 12.16. Variable output resistance of inverted R-2R ladder in CMOS DACs.

If  $R = 10\text{ k}\Omega$ , the resistance looking back into the network is about  $10\text{ k}\Omega$  for codes containing more than about four 1's, and  $30\text{ k}\Omega$  for a single 1. Thus, for the one-bit transition from 0011 1111 1111 to 0100 0000 0000, the error voltage,  $V_{os} (1 + R_F/R_o)$ , changes from  $2 V_{os}$  to  $(4/3) V_{os}$ . If the offset had been nulled by current summation at all-zeros ( $1 + R_F/R_o = 1$ , since  $R_o \rightarrow \infty$ ), the offset error will be  $+V_{os}$  at the first code and  $+(1/3) V_{os}$  at the second code; the incremental change of error will be  $(-2/3) V_{os}$ . If  $V_{os}$  is not much smaller than the voltage equivalent of the least-significant bit (see Table 12.1), differential nonlinearity errors can result in nonmonotonic behavior.

The solution to this dilemma is simple: use (a) for zeroing the amplifier. Better yet, use an amplifier having extremely low offset and negligible bias current.

“Foreign” currents in common ground and power lines can introduce offset, noise, and other errors that will be amplified in the same way as  $V_{os}$  errors.

It is important to refer the amplifier circuit (and its external  $V_{os}$  trim), the load across which the output voltage is being developed, and the DAC's reference input—all of these—to the DAC terminals, in the manner shown in Figure 12.17.

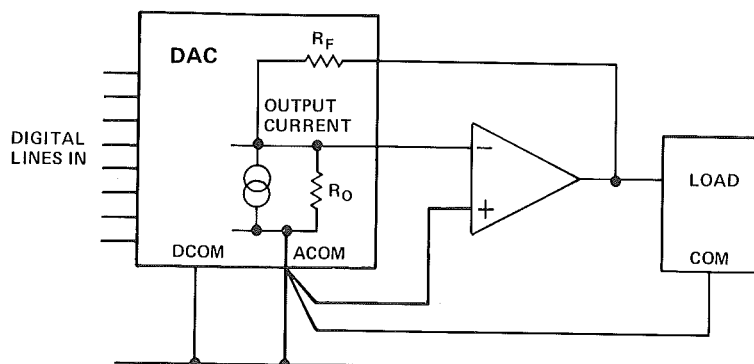


Figure 12.17. Referring buffer amplifier and load circuits to analog common.

### 12.4.2 MORE ON BYPASSING AND GROUNDING

In “virtual-ground” systems, such as an op amp, driven by a current-output DAC, the DAC output current doesn't actually return to ground, but to one of the power supplies, by way of the op amp's output stage (Figure 12.18). To reduce the impedance in the high-frequency current path, the bypass capacitor should be connected so as to return the currents from one (or both) power terminals to ground *at the DAC*. If the DAC output is active, it may require bypassing of its own supplies for the same reason.

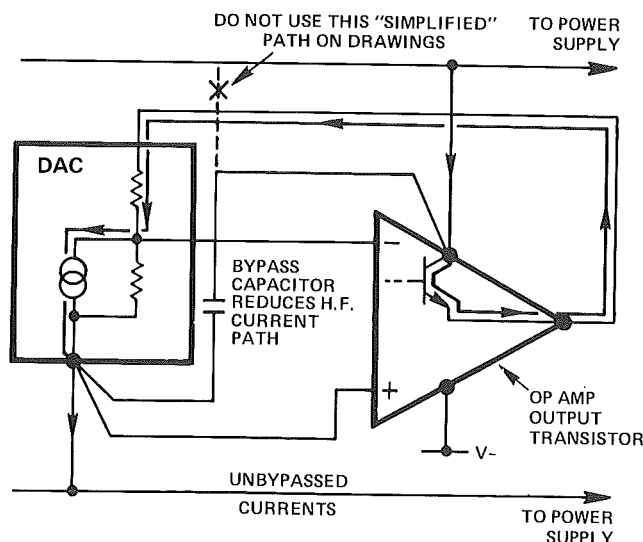


Figure 12.18. Bypassing power supplies for virtual-ground applications. Arrows show unypassed current flow.

**WARNING:** You and your drafting department may have conflicting objectives. Your objective is to design circuits that work and communicate the important details to whoever assembles them. Your drafting department (or so it may often seem) has the objective of drawing nice, neat, squared-off diagrams, in which the lines representing conductors are remarkably equipotential. You may have noticed that, where it counts in Figures 12.17 and 12.18, these niceties have been avoided. The lines are configured to resemble closely the job that the wires perform, converging at the common analog connection.

For example, the bypass lead, in Figure 12.18, though artistically squared off, wends its way purposefully in the direction of the op-amp's power-supply terminal, rather than shooting straight up to meet the power-supply line (a sure recipe for costly debugging). If you think your drafting department may have a mind of its own, you may want to include a special message for the person who builds the circuit, to be sure that it gets built the way you want it built. If you have a computer-aided-engineering setup that allows you to create drawings that directly reflect your wishes, this is one less matter for you to worry about.

Figure 12.19a shows an example of ineffective decoupling. Here the op amp drives a load, which connects to a long ground line (returning to the power-supply terminal), and the supply decoupling for the amplifier returns to the power supply through another long line. The return path for the load current is as long as, or longer than, the supply lines powering the op amp. The "local" decoupling is not only ineffective; it may actually contribute to noise on the power-ground bus.

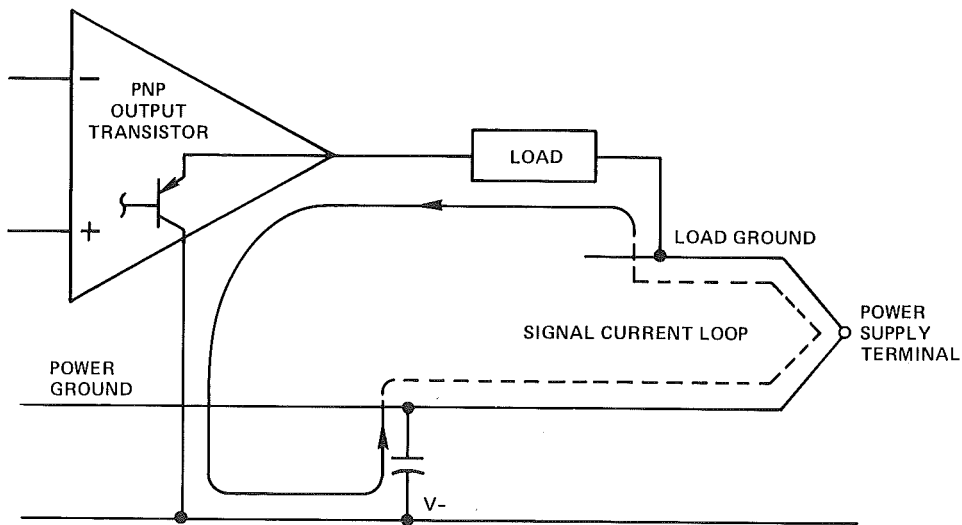
The cardinal rule of decoupling is:

**Make it easy for the current to get back by the shortest path.**

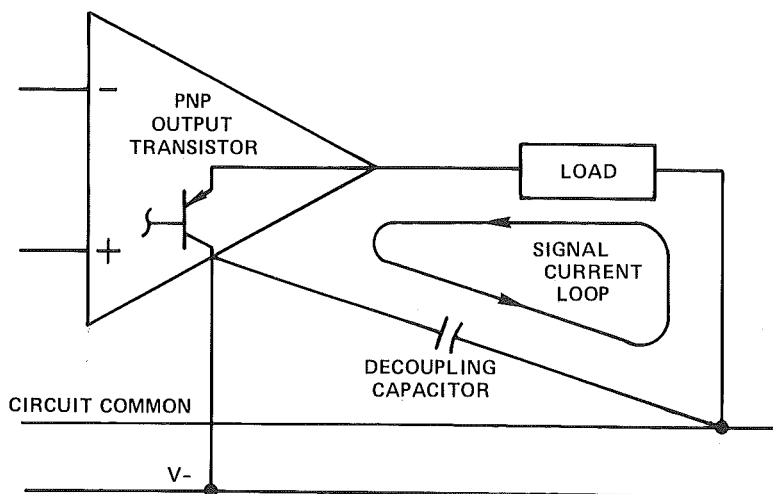
Figure 12.19b shows a more effective scheme, in which the decoupling capacitor connects by the shortest path between the load return and the load-voltage control element. Here an op amp, swinging a resistive load-circuit negative, drives the load from an internal PNP transistor, connected to  $V^-$ . Decoupling the  $V^-$  pin of the op amp to the low side of the load provides the most direct return path for high-frequency currents and bypasses them around ground and power buses.

Well-designed data sheets will offer specific suggestions for grounding and/or decoupling. For example, the data sheet for the Analog Devices AD390 quad 12-bit d/a converter suggests: "The power supplies used with the AD390 should be well filtered and regulated. Local supply decoupling, consisting of a 10- $\mu$ F tantalum capacitor in parallel with 0.1- $\mu$ F ceramic, is suggested. The decoupling capacitors should be connected between the AD390 supply pins and the load ground (ideally the AGND pin). If an output booster is used, its supplies should also be decoupled to the load ground."





a. Decoupling for negative supply is ineffective.



b. Decoupling of negative supply is optimized for "grounded" load.

Figure 12.19. Effective and ineffective decoupling.

### Substitutes for Ground

In large systems, it is often impractical to rely on a single common point for all analog signals. In these cases, some form of differential (or even *isolation*) amplifier is required to translate signals between ground systems. For the inveterate op-amp user, a simple subtractor, or “dynamic bridge” circuit may come to mind. These circuits translate a signal which is referred to one ground system into a similar or amplified signal, referred to a different ground signal (Figure 12.20). The common-mode rejection of the amplifier and a resistance-ratio match are used to eliminate the effects of voltage differences between the two grounds, or common points.

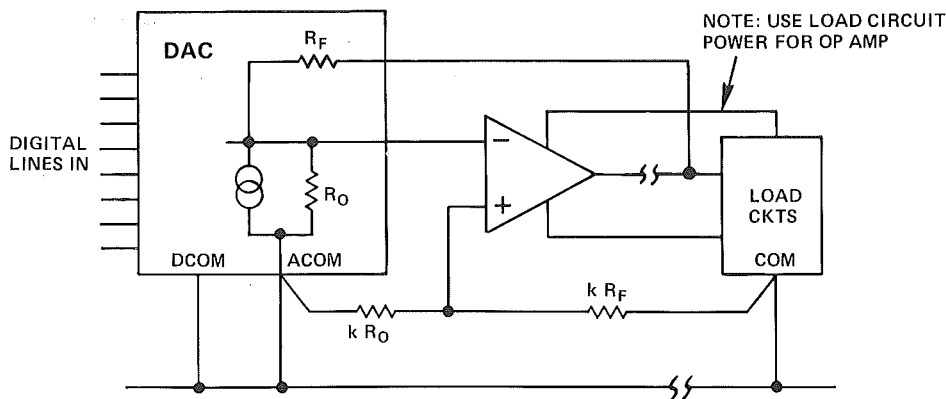


Figure 12.20. Use of differential amplifier to eliminate the effects of common-mode voltage.

It is generally wise to power the op amp from the power available at the *load* side of the circuit, and/or to decouple it with respect to the *load* common. The reason for this can be deduced from the circuit architecture of the most-common types of op amps (Figure 12.21).

An op amp converts a differential input signal to a single-ended output signal. In many popular op amps, the differential-to-single-ended conversion is done with respect to  $V^-$  (but some use  $V^+$ ), and the resulting signal drives an integrator<sup>2</sup>. The integrator characteristic is used to frequency-compensate the amplifier, and the integrator input is referred to the single-ended output, at  $V^-$ . The integrator acts as a unity-gain follower for fast signals applied to its non-inverting (or reference) input. As a result, signals applied to the  $V^-$  terminal have their high-frequency components conveyed directly to the output. Signals having frequency components *above* the amplifier's *closed-loop* bandwidth will be transmitted from  $V^-$  to the output with little or no attenuation.

<sup>2</sup>The Application Note mentioned in footnote (1), “An I.C. Amplifier User’s Guide to Decoupling, Grounding, and Making Things Go Right for a Change,” provides considerable detail regarding the integrator-reference and compensation schemes of more than 40 device families.

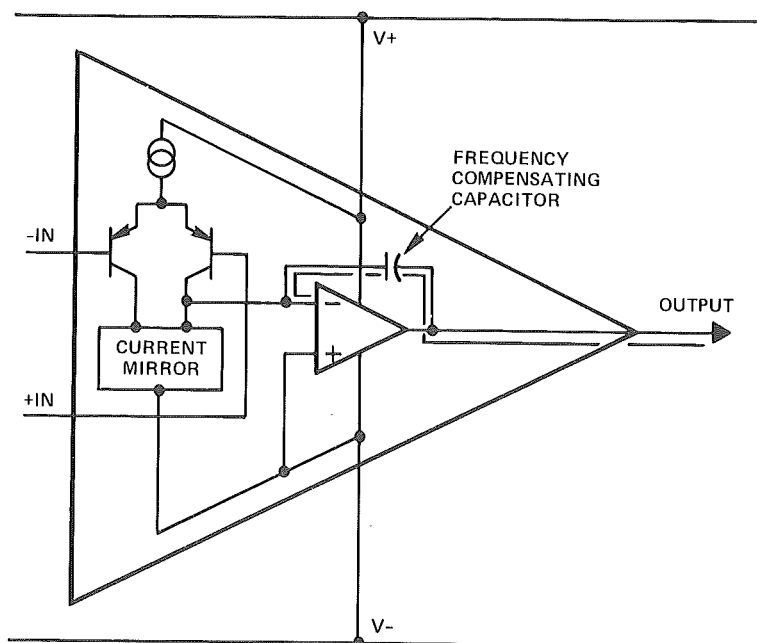


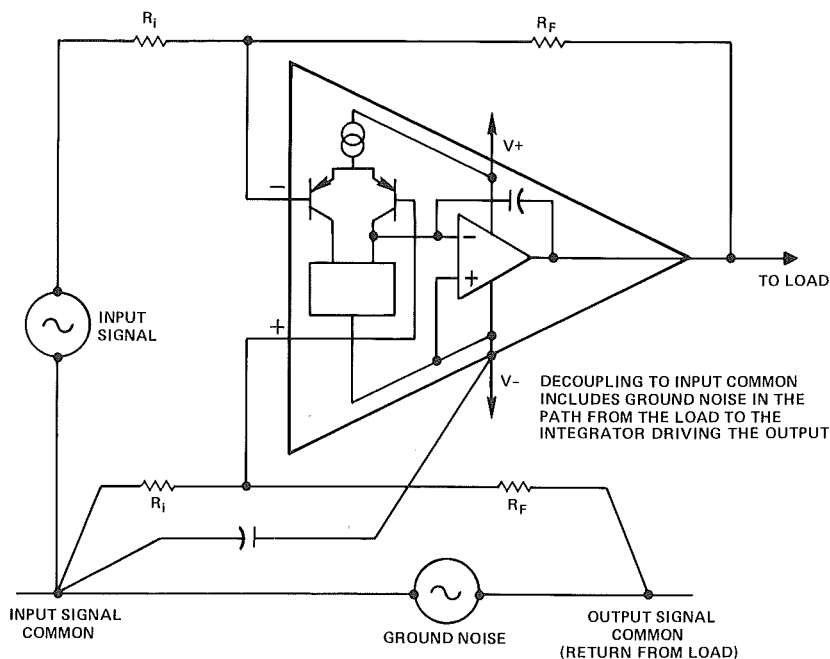
Figure 12.21. Typical op-amp circuit architecture. Reference for output integrator is  $V_-$ .

As Figure 12.22a shows, if the op amp used as a subtractor amplifier is powered from or bypassed to the same common line as the input signal, any high-frequency signals associated with the common will appear as part of the output signal. If the ground noise includes appreciable high-frequency noise (such as are produced by logic currents), the common-mode rejection will be defeated.

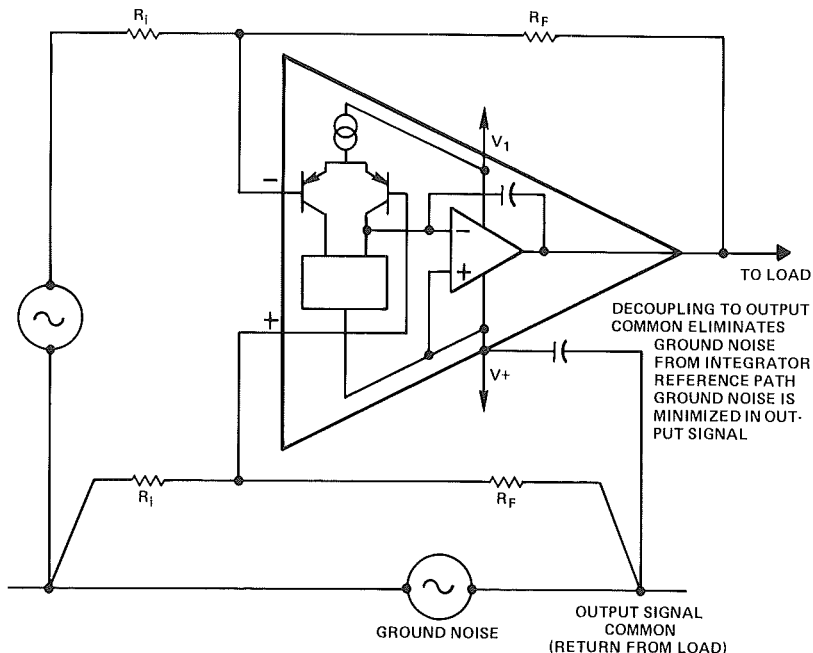
If, on the other hand (Figure 12.22b), the op-amp supply terminals are referred to the *output* signal common, no extraneous signals are coupled into the integrator. Any ground noise appears as a common-mode input signal and is reduced by the common-mode rejection of the amplifier (which is typically very much better than the negative-supply rejection at high frequencies).

Since noise-rejection performance of the subtractor depends on carefully matched source and feedback resistance ratios, it cannot be used in all situations. Whenever the source impedance cannot be controlled, or is exceptionally high, the subtractor (or dynamic bridge) becomes impractical. In this situation, ground noise and other remote-grounding difficulties can often be avoided by the use of an *instrumentation amplifier*.

IC instrumentation amplifiers, such as the AD524, accept differential input signals at high impedance, provide a fixed gain (which can be selected without introducing overall feedback that joins the input and output circuitry), and develop the output voltage with respect to a reference terminal, which may be connected to the input common of a remote load circuit (Figure 12.23).



a. Decoupling to *input* common includes ground noise in the path from the load to the integrator driving the output.



b. Decoupling to *output* common eliminates ground noise from the integrator reference path. Ground noise is minimized in the output signal.

Figure 12.22. Proper and improper decoupling of subtractors using op amp with integrator referred to  $V_-$ .

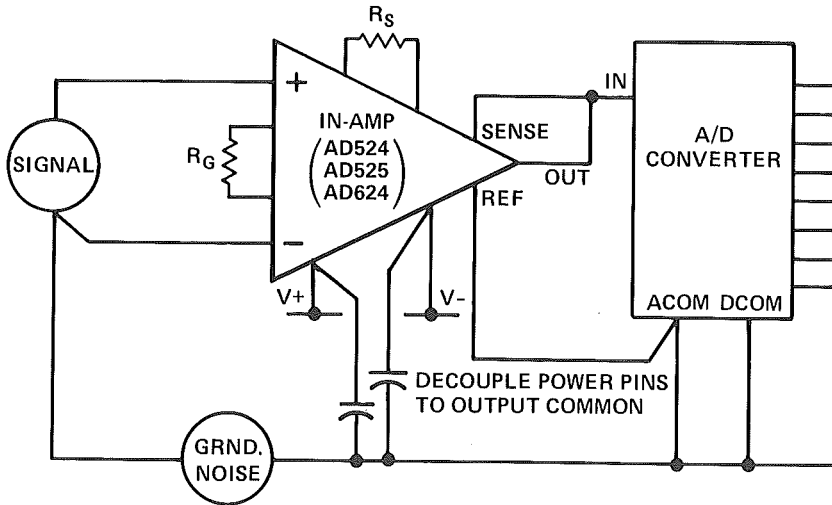


Figure 12.23. Instrumentation amplifier interfaces separate ground systems.

Some instrumentation amplifiers are quite versatile and can provide additional functions, while isolating the common returns. For example, the output-reference terminal can be used to add a fixed or variable bias voltage to the output.

If the common-mode voltages are very large, or if galvanic isolation is essential for safety, isolation amplifiers—or amplifiers powered by isolated dc-to-dc converters—may be highly desirable.

